CC1311R3 SimpleLink™ High-Performance Sub-1 GHz Wireless MCU

1 Features

Wireless microcontroller

- Powerful 48-MHz Arm® Cortex®-M4 processor
- 352KB flash program memory
- 32KB of ultra-low leakage SRAM
- 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
- Programmable radio includes support for 2-(G)FSK, 4-(G)FSK, MSK, OOK, IEEE 802.15.4 PHY and MAC
- Supports over-the-air upgrade (OTA)

Low power consumption

- MCU consumption:
  - 2.63 mA active mode, CoreMark®
  - 55 µA/MHz running CoreMark
  - 0.7 µA standby mode, RTC, 32KB RAM
  - 0.1 µA shutdown mode, wake-up on pin
- Radio Consumption:
  - 5.4 mA RX at 868 MHz
  - 24.9 mA TX at +14 dBm at 868 MHz

Wireless protocol support

- mioty
- Wireless M-Bus
- SimpleLink™ TI 15.4-stack
- 6LoWPAN
- Proprietary systems

High performance radio

- -121 dBm for 2.5-kbps long-range mode
- -120 dBm at 4.8 kbps narrowband mode, 433 MHz
- -118 dBm at 9.6 kbps narrowband mode, 868 MHz
- -110 dBm at 50 kbps, 802.15.4, 868 MHz
- Output power up to +14 dBm with temperature compensation
- Down to 4 kHz receiver filter bandwidth

Regulatory compliance

- Suitable for systems targeting compliance with these standards:
  - ETSI EN 300 220 Receiver Cat. 1.5 and 2, EN 303 131, EN 303 204
  - FCC CFR47 Part 15
  - ARIB STD-T108

MCU peripherals

- Digital peripherals can be routed to any GPIO
- Four 32-bit or eight 16-bit general-purpose timers
- 12-bit ADC, 200 kSamples/s, 8 channels
- 8-bit DAC
- Analog Comparator
- UART, SSI, I^2C, I^2S
- Real-time clock (RTC)
- Integrated temperature and battery monitor

Security enablers

- AES 128-bit cryptographic accelerator
- True random number generator (TRNG)
- Additional cryptography drivers available in Software Development Kit (SDK)

Development tools and software

- LP-CC1311P3 Development Kit
- SimpleLink™ CC13xx and CC26xx Software Development Kit (SDK)
- SmartRF™ Studio for simple radio configuration
- SysConfig system configuration tool

Operating range

- On-chip buck DC/DC converter
- 1.8-V to 3.8-V single supply voltage
- -40 to +105°C

Package

- 7-mm × 7-mm RGZ VQFN48 (30 GPIOs)
- 5-mm × 5-mm RKP VQFN40 (22 GPIOs)
- RoHS-compliant package

2 Applications

- Grid infrastructure
  - Smart Meters – electricity meter, water meter, gas meter, and heat cost allocator
  - Grid communications – wireless communications
  - EV charging infrastructure – AC charging (pile) station
  - Other alternative energy – energy harvesting
- Building automation
  - Building security systems – motion detector, door and window sensor, glass break detector, panic button, electronic smart lock and IP network camera
  - HVAC systems – thermostat, environmental sensor and HVAC controller
  - Fire safety – smoke and head detector, gas detector and fire alarm control panel
- Retail Automation
  - Retail automation & payment applications – electronic shelf labels andportable POS terminal
- Personal Electronics
  - RF remote controls
  - Smart Speakers and Smart Displays
  - Gaming and electronic and robotic toys
  - Wearables (non-medical) and smart trackers
- Wireless Modules
  - Wireless third party modules
  - Wireless communications modules

3 Description

The SimpleLink™ CC1311R3 device is a multiprotocol Sub-1 GHz wireless microcontroller (MCU) supporting IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), mioty, proprietary systems, including the TI 15.4-Stack (Sub-1 GHz). The CC1311R3 is based on an Arm® Cortex® M4 main processor and optimized for low-power wireless communication and advanced sensing in grid infrastructure, building automation, retail automation, personal electronics and medical applications.

The CC1311R3 has a software defined radio powered by an Arm® Cortex® M0, which allows support for multiple physical layers and RF standards. The device supports operation in 143 to 176-MHz, 287 to 351-MHz, 359 to 527-MHz, 861 to 1054-MHz, and 1076 to 1315-MHz frequency bands. The CC1311R3 has an efficient built-in PA that supports +14 dBm TX at 24.9 mA current consumption. In RX it has -121 dBm sensitivity and 88 dB blocking ±10 MHz in SimpleLink™ long-range mode with 2.5-kbps data rate.

The CC1311R3 has a low sleep current of 0.7 µA with RTC and 32KB RAM retention.

Consistent with many customers' 10 to 15 years or longer life cycle requirements, TI has a product life cycle policy with a commitment to product longevity and continuity of supply.

The CC1311R3 device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, *Bluetooth*® Low Energy, Thread, Zigbee, Wi-SUN®, Amazon Sidewalk, mioty, Sub-1 GHz MCUs, and host MCUs. CC1311R3 is part of a scalable portfolio with flash sizes from 32KB to 704KB with pin-to-pin compatible package options. The common SimpleLink™CC13xx and CC26xx Software Development Kit (SDK) and SysConfig system configuration tool supports migration between devices in the portfolio. A comprehensive number of software stacks, application examples and SimpleLink™ Academy training sessions are included in the SDK. For more information, visit wireless connectivity.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
CC1311R31T0RGZR	VQFN (48)	7.00 mm × 7.00 mm
CC1311R31T0RKPR	VQFN (40)	5.00 mm × 5.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in Section 12, or see the TI website.

4 Functional Block Diagram

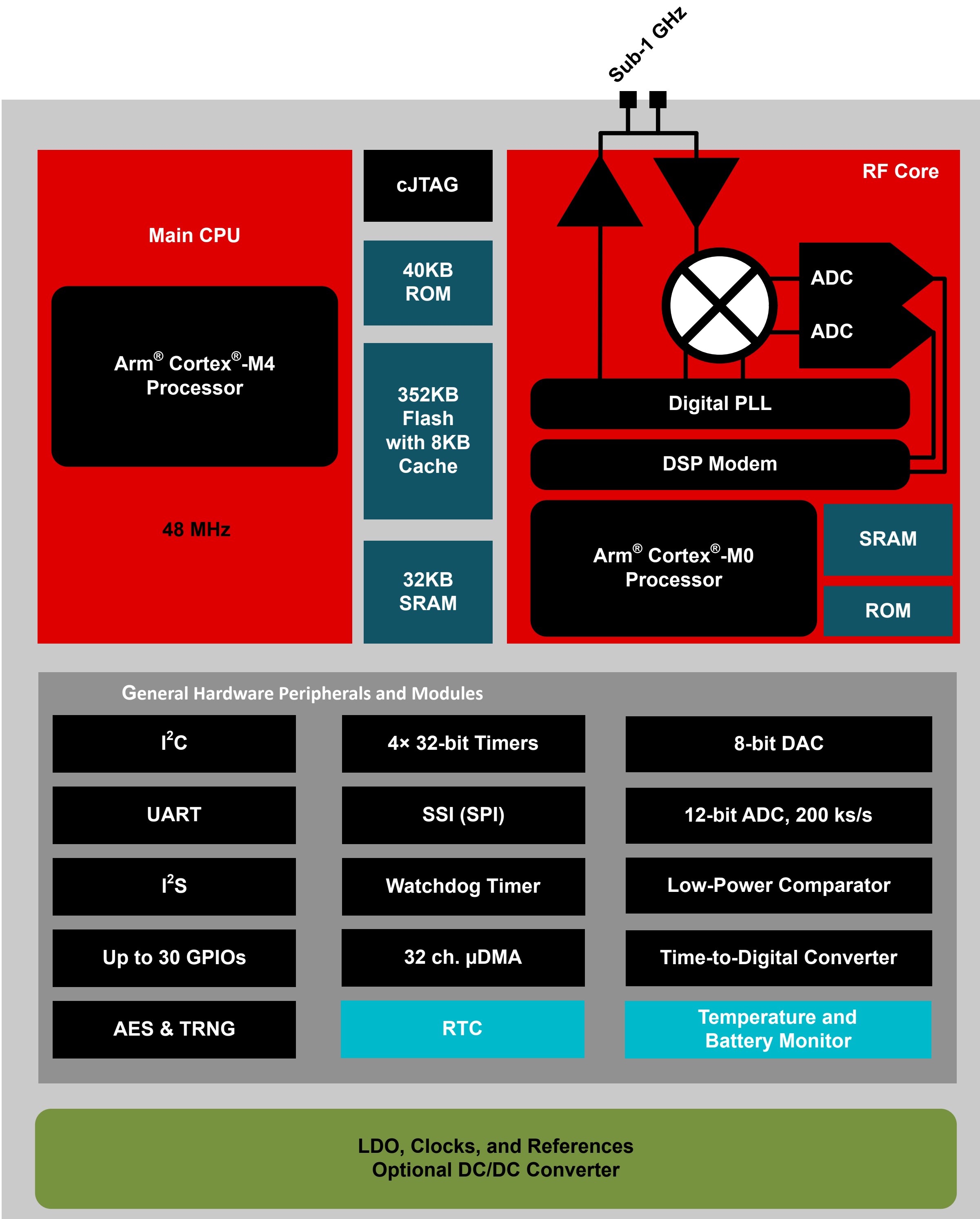

Figure 4-1. CC1311R3 Functional Block Diagram

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial Release

6 Device Comparison

Device	RADIO SUPPORT											FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE			
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	mioty	Wi-SUN®	Sidewalk	*Bluetooth®* 5.2 LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 X 4 mm VQFN (32)	5 X 5 mm VQFN (32)	5 X 5 mm VQFN (40)	7 X 7 mm VQFN (48)
CC1310	X		X	X								32-128	16-20 + 8	10-30	X	X		X
CC1311R3	X		X	X								352	32 + 8	22-30			X	X
CC1311P3	X		X	X							X	352	32 + 8	26				X
CC1312R	X		X	X	X							352	80 + 8	30				X
CC1312R7	X		X	X	X	X				X		704	144 + 8	30				X
CC1352R	X	X	X	X	X		X	X	X	X		352	80 + 8	28				X
CC1352P	X	X	X	X	X		X	X	X	X	X	352	80 + 8	26				X
CC1352P7	X	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26				X
CC2640R2F							X					128	20 + 8	10-31	X	X		X
CC2642R							X					352	80 + 8	31				X
CC2642R-Q1							X					352	80 + 8	31				X
CC2651R3		X					X	X				352	32 + 8	23-31			X	X
CC2651P3		X					X	X			X	352	32 + 8	22-26			X	X
CC2652R		X					X	X	X	X		352	80 + 8	31				X
CC2652RB		X					X	X	X	X		352	80 + 8	31				X
CC2652R7		X					X	X	X	X		704	144 + 8	31				X
CC2652P		X					X	X	X	X	X	352	80 + 8	26				X
CC2652P7		X					X	X	X	X	X	704	144 + 8	26				X

7 Pin Configuration and Functions

7.1 Pin Diagram – RGZ Package (Top View)

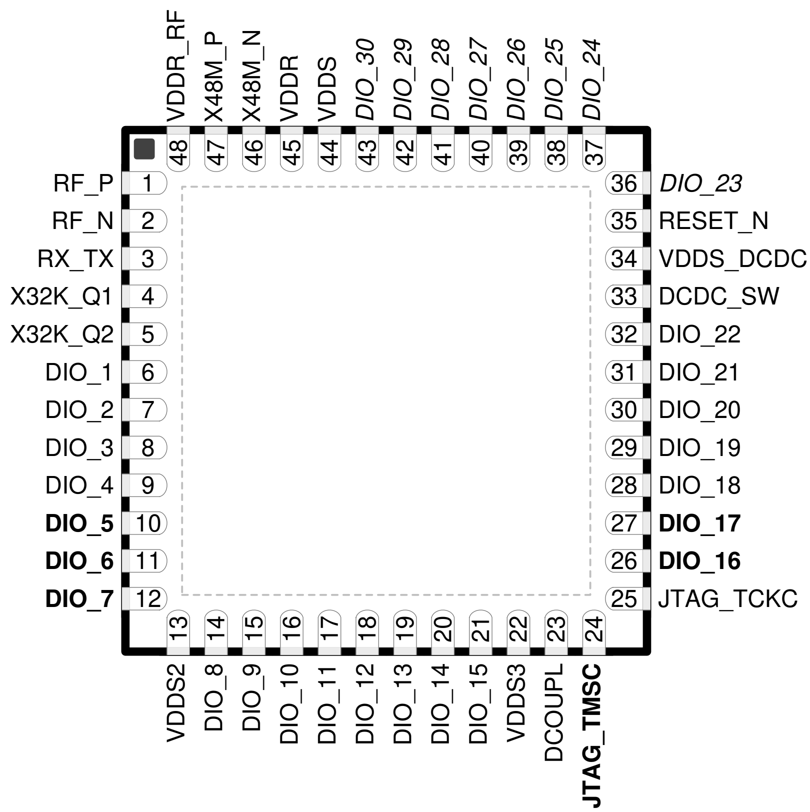

Figure 7-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in Figure 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in Figure 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

7.2 Signal Descriptions – RGZ Package

Table 7-1. Signal Descriptions – RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter[(1)]
DCOUPL	23	—	Power	For decoupling of internal 1.27 V regulated digital-supply [(2)]
DIO_1	6	I/O	Digital	GPIO
DIO_2	7	I/O	Digital	GPIO
DIO_3	8	I/O	Digital	GPIO
DIO_4	9	I/O	Digital	GPIO
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, analog capability
DIO_24	37	I/O	Digital or Analog	GPIO, analog capability
DIO_25	38	I/O	Digital or Analog	GPIO, analog capability
DIO_26	39	I/O	Digital or Analog	GPIO, analog capability
DIO_27	40	I/O	Digital or Analog	GPIO, analog capability
DIO_28	41	I/O	Digital or Analog	GPIO, analog capability
DIO_29	42	I/O	Digital or Analog	GPIO, analog capability
DIO_30	43	I/O	Digital or Analog	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad[(3)]
JTAG_TMSC	24	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCKC
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	3	—	RF	Optional bias pin for the RF LNA
VDDR	45	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO[(2)] [(4)] [(6)]

Table 7-1. Signal Descriptions – RGZ Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR_RF	48	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (5) (6)
VDDS	44	—	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	22	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	34	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	46	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	47	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	4	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	5	—	Analog	32-kHz crystal oscillator pin 2

(1) For more details, see the device technical reference manual listed in Section 11.3.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.3 Pin Diagram – RKP Package (Top View)

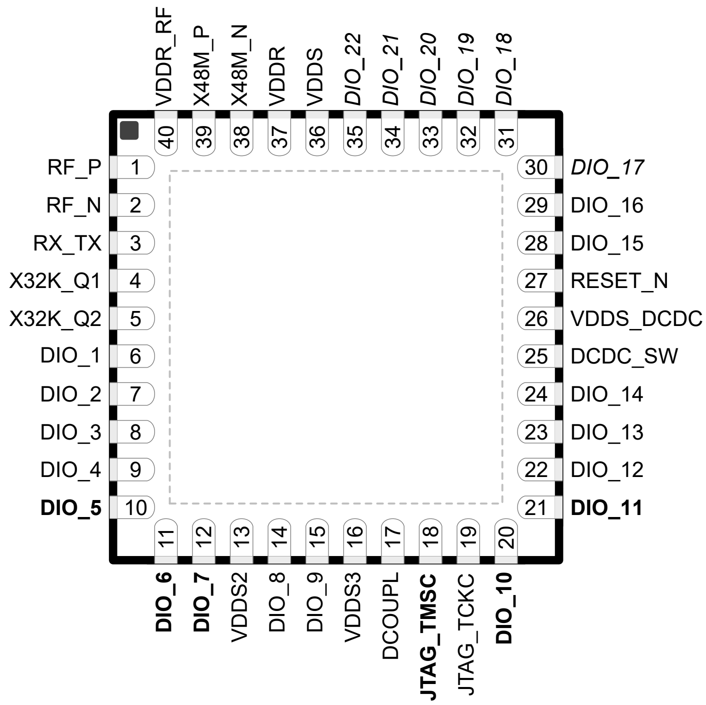

Figure 7-2. RKP (5-mm × 5-mm) Pinout, 0.4-mm Pitch (Top View)

The following I/O pins marked in Figure 7-2 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 18, JTAG_TMSC
- Pin 20, DIO_10
- Pin 21, DIO_11

The following I/O pins marked in Figure 7-2 in *italics* have analog capabilities:

- Pin 28, DIO_15
- Pin 29, DIO_16
- Pin 30, DIO_17
- Pin 31, DIO_18
- Pin 32, DIO_19
- Pin 33, DIO_20
- Pin 34, DIO_21
- Pin 35, DIO_22

7.4 Signal Descriptions – RKP Package

Table 7-2. Signal Descriptions – RKP Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	25	—	Power	Output from internal DC/DC converter[(1)]
DCOUPL	17	—	Power	For decoupling of internal 1.27 V regulated digital-supply [(2)]
DIO_1	6	I/O	Digital	GPIO
DIO_2	7	I/O	Digital	GPIO
DIO_3	8	I/O	Digital	GPIO

Table 7-2. Signal Descriptions – RKP Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DIO_4	9	I/O	Digital	GPIO
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	20	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_11	21	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_12	22	I/O	Digital	GPIO
DIO_13	23	I/O	Digital	GPIO
DIO_14	24	I/O	Digital	GPIO
DIO_15	28	I/O	Digital	GPIO, analog capability
DIO_16	29	I/O	Digital	GPIO, analog capability
DIO_17	30	I/O	Digital	GPIO, analog capability
DIO_18	31	I/O	Digital	GPIO, analog capability
DIO_19	32	I/O	Digital	GPIO, analog capability
DIO_20	33	I/O	Digital	GPIO, analog capability
DIO_21	34	I/O	Digital	GPIO, analog capability
DIO_22	35	I/O	Digital	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad(3)
JTAG_TSMC	18	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	19	I	Digital	JTAG TCKC
RESET_N	27	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	3	—	RF	Optional bias pin for the RF LNA
VDDR	37	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (4) (6)
VDDR_RF	40	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (5) (6)
VDDS	36	—	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	16	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	26	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	38	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	39	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	4	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	5	—	Analog	32-kHz crystal oscillator pin 2

(1) For more details, see the device technical reference manual listed in Section 11.3.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.5 Connections for Unused Pins and Modules

Table 7-3. Connections for Unused Pins – RGZ Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO	DIO_n	6–12 14–21 26–32 36–43	NC or GND	NC
32.768-kHz crystal	X32K_Q1	4	NC or GND	NC
	X32K_Q2	5		
DC/DC converter(2)	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 uF DCDC capacitor must be kept on the VDDR net.

Table 7-4. Connection for Unused Pins and Modules – RKP Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE	PREFERRED PRACTICE
GPIO	DIO_n	6-12 14-15 20-24 28-35	NC or GND	NC
32.768-kHz crystal	X32K_Q1	3	NC or GND	NC
	X32K_Q2	4		
No Connects	NC		NC	NC
DC/DC converter	DCDC_SW	25	NC	NC
	VDDS_DCDC	26	VDDS	VDDS

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

			MIN	MAX	UNIT
VDDS[(3)]	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin[(4)] [(5)]		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input level, RF pins (RF_P and RF_N)			10	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.
(5) Injection current is not supported on any GPIO pin

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating ambient temperature[(1)] [(2)]		–40	105	°C
Operating junction temperature[(1)] [(2)]		–40	115	°C
Operating supply voltage (VDDS)		1.8	3.8	V
Operating supply voltage (VDDS), boost mode	VDDR = 1.95 V +14 dBm RF output power	2.1	3.8	V
Rising supply voltage slew rate		0	100	mV/µs
Falling supply voltage slew rate[(3)]		0	20	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in lifetime reduction.
(2) For thermal resistance characteristics refer to Section 8.8.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.

8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VDDS Power-on-Reset (POR) threshold			1.1 - 1.55		V
VDDS Brown-out Detector (BOD) [(1)]	Rising threshold		1.77		V
VDDS Brown-out Detector (BOD), before initial boot [(2)]	Rising threshold		1.70		V
VDDS Brown-out Detector (BOD) [(1)]	Falling threshold		1.75		V

(1) For boost mode (VDDR =1.95 V), TI drivers software initialization will trim VDDS BOD limits to maximum (approximately 2.0 V)

(2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

8.5 Power Consumption - Power Modes

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.6 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	115	nA
		Shutdown. No clocks running, no retention	115	
	Standby without cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF	0.7	µA
		RTC running, CPU, 32KB RAM and (partial) register retention XOSC_LF	0.8	µA
	Standby with cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF	2.1	µA
		RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF	2.2	µA
	Idle	Supply Systems and RAM powered RCOSC_HF	570	µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF	2.50	mA
Peripheral Current Consumption				
I_{peri}	Peripheral power domain	Delta current with domain enabled	47.0	µA
	Serial power domain	Delta current with domain enabled	3.3	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	122	
	µDMA	Delta current with clock enabled, module is idle	58.1	
	Timers	Delta current with clock enabled, module is idle[(1)]	87.0	
	I2C	Delta current with clock enabled, module is idle	11.6	
	I2S	Delta current with clock enabled, module is idle	25.8	
	SSI	Delta current with clock enabled, module is idle	61.3	
	UART	Delta current with clock enabled, module is idle	125	
	CRYPTO (AES)	Delta current with clock enabled, module is idle	25.2	
	TRNG	Delta current with clock enabled, module is idle	23.3	

(1) Only one GPTimer running

8.6 Power Consumption - Radio Modes

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.6 V with DC/DC enabled unless otherwise noted.
Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14 dBm setting where this current is already included).
Relevant I_{core} and I_{peri} currents are included in below numbers.

PARAMETER		TEST CONDITIONS	TYP	UNIT
	Radio receive current, 868 MHz		5.4	mA
	Radio transmit current	0 dBm output power setting 868 MHz	7.4	mA
		+10 dBm output power setting 868 MHz	13.9	mA
	Radio transmit current Boost mode	+14 dBm output power setting 868 MHz	24.9	mA

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank[(1) (5)]		30			k Cycles
Supported flash erase cycles before failure, single sector[(2)]		60			k Cycles
Maximum number of write operations per row before sector erase[(3)]				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash sector erase current	Average delta current		9.7		mA
Flash sector erase time[(4)]	Zero cycles		10		ms
	30k cycles			4000	ms
Flash write current	Average delta current, 4 bytes at a time		5.3		mA
Flash write time[(4)]	4 bytes at a time		21.6		µs

(1) A full bank erase is counted as a single erase cycle on each sector.
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

THERMAL METRIC[(1)]		PACKAGE		UNIT
		RGZ (VQFN)	RKP (VQFN)	
		48 PINS	40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.0	30.9	°C/W[(2)]
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	20.2	°C/W[(2)]
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	10.3	°C/W[(2)]
Ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W[(2)]
Ψ_{JB}	Junction-to-board characterization parameter	8.6	10.3	°C/W[(2)]
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	2.1	°C/W[(2)]

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	1076		1315	MHz
	861		1054	
	431		527	
	359		439	
	287		351	
	143		176	

8.10 861 MHz to 1054 MHz - Receive (RX)

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Digital channel filter programmable receive bandwidth		4		4000	kHz
Data rate step size			1.5		bps
Spurious emissions 25 MHz to 1 GHz	868 MHz Conducted emissions measured according to ETSI EN 300 220		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		dBm
IEEE 802.15.4, 50 kbps, ±25 kHz Deviation, 2-GFSK, 100 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		–110		dBm
Saturation limit	BER = 10^{-2}, 868 MHz		10		dBm
Selectivity, ±200 kHz	BER = 10^{-2}, 868 MHz[1]		44		dB
Selectivity, ±400 kHz	BER = 10^{-2}, 868 MHz[1]		48		dB
Blocking, ±1 MHz	BER = 10^{-2}, 868 MHz[1]		58		dB
Blocking, ±2 MHz	BER = 10^{-2}, 868 MHz[1]		62		dB
Blocking, ±5 MHz	BER = 10^{-2}, 868 MHz[1]		70		dB
Blocking, ±10 MHz	BER = 10^{-2}, 868 MHz[1]		77		dB
Image rejection (image compensation enabled)	BER = 10^{-2}, 868 MHz[1]		41		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
100 kbps, ±25 kHz Deviation, 2-GFSK, 137 kHz RX Bandwidth					
Sensitivity 100 kbps	1% PER, 127 byte payload, 868 MHz		-104		dBm
Selectivity, ±200 kHz	1% PER, 127 byte payload, 868 MHz. Wanted signal at -96 dBm		31		dB
Selectivity, ±400 kHz	1% PER, 127 byte payload, 868 MHz. Wanted signal at -96 dBm		37		dB
Co-channel rejection	1% PER, 127 byte payload, 868 MHz. Wanted signal at -79 dBm		-9		dB
200 kbps, ±50 kHz Deviation, 2-GFSK, 311 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		–103		dBm
Sensitivity	BER = 10^{-2}, 915 MHz		–102		dBm
Selectivity, ±400 kHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		45		dB
Selectivity, ±800 kHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		49		dB
Blocking, ±2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		57		dB
Blocking, ±10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		69		dB
500 kbps, ±190 kHz Deviation, 2-GFSK, 1150 kHz RX Bandwidth					
Sensitivity 500 kbps	1% PER, 127 byte payload, 915 MHz		-94		dBm
Selectivity, ±1 MHz	1% PER, 127 byte payload, 915 MHz. Wanted signal at -88 dBm		14		dB
Selectivity, ±2 MHz	1% PER, 127 byte payload, 915 MHz. Wanted signal at -88 dBm		42		dB
Co-channel rejection	1% PER, 127 byte payload, 915 MHz. Wanted signal at -71 dBm		-9		dB
1 Mbps, ±350 kHz Deviation, 2-GFSK, 1.3 MHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		-97		dBm
Sensitivity	BER = 10^{-2}, 915 MHz		-96		dBm
Blocking, +2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		43		dB
Blocking, -2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		26		dB
Blocking, +10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		54		dB
Blocking, -10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		48		dB
SimpleLink™ Long Range, 2.5/5 kbps (20 ksps), ±5 kHz Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = 10^{-2}, 868 MHz		-121		dBm
Sensitivity	5 kbps, BER = 10^{-2}, 868 MHz		-119		dBm
Saturation limit	2.5 kbps, BER = 10^{-2}, 868 MHz		10		dBm
Selectivity, ±100 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[1]		49		dB

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±200 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		50		dB
Selectivity, ±300 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		51		dB
Blocking, ±1 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		63		dB
Blocking, ±2 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		69		dB
Blocking, ±5 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		79		dB
Blocking, ±10 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		88		dB
Image rejection (image compensation enabled)	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		47		dB
RSSI dynamic range	Starting from the sensitivity limit		97		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
Narrowband, 9.6 kbps, ±2.4 kHz Deviation, 2-GFSK, 17.1 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		-117		dBm
Adjacent Channel Rejection	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm). Interferer ±20 kHz		41		dB
Alternate Channel Rejection	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm). Interferer ±40 kHz		42		dB
Blocking, ±1 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		65		dB
Blocking, ±2 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		70		dB
Blocking, ±10 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		85		dB
Wi-SUN, 2-GFSK					
Sensitivity	50 kbps, ±12.5 kHz deviation, 2-GFSK, 68 kHz RX Bandwidth, 868 MHz, 10% PER, 250 byte payload		-107		dBm
Selectivity, ±100 kHz, 50 kbps, ±12.5 kHz deviation, 2-GFSK, 868.3 MHz	50 kbps, ±12.5 kHz deviation, 2-GFSK, 68 kHz RX Bandwidth, 868.3 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		30		dB
Selectivity, ±200 kHz, 50 kbps, ±12.5 kHz deviation, 2-GFSK, 868.3 MHz	50 kbps, ±12.5 kHz deviation, 2-GFSK, 68 kHz RX Bandwidth, 868.3 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		36		dB
Sensitivity	50 kbps, ±25 kHz deviation, 2-GFSK, 98 kHz RX Bandwidth, 918.2 MHz, 10% PER, 250 byte payload		-106		dBm
Selectivity, ±200 kHz, 50 kbps, ±25 kHz deviation, 2-GFSK, 918.2 MHz	50 kbps, ±25 kHz deviation, 2-GFSK, 98 kHz RX Bandwidth, 918.2 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		34		dB
Selectivity, ±400 kHz, 50 kbps, ±25 kHz deviation, 2-GFSK, 918.2 MHz	50 kbps, ±25 kHz deviation, 2-GFSK, 98 kHz RX Bandwidth, 918.2 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		41		dB
Sensitivity	100 kbps, ±25 kHz deviation, 2-GFSK, 135 kHz RX Bandwidth, 868 MHz, 10% PER, 250 byte payload		-104		dBm
Selectivity, ±200 kHz, 100 kbps, ±25 kHz deviation, 2-GFSK, 868.3 MHz	100 kbps, ±25 kHz deviation, 2-GFSK, 135 kHz RX Bandwidth, 868.3 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		37		dB
Selectivity, ±400 kHz, 100 kbps, ±25 kHz deviation, 2-GFSK, 868.3 MHz	100 kbps, ±25 kHz deviation, 2-GFSK, 135 kHz RX Bandwidth, 868.3 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		45		dB
Sensitivity	100 kbps, ±50 kHz deviation, 2-GFSK, 196 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload		-102		dBm
Selectivity, ±400 kHz, 100 kbps, ±50 kHz deviation, 2-GFSK, 920.9 MHz	100 kbps, ±50 kHz deviation, 2-GFSK, 196 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		40		dB
Selectivity, ±800 kHz, 100 kbps, ±50 kHz deviation, 2-GFSK, 920.9 MHz	100 kbps, ±50 kHz deviation, 2-GFSK, 196 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		49		dB
Sensitivity	150 kbps, ±37.5 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload		-99		dBm

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±400 kHz, 150 kbps, ±37.5 kHz deviation, 2-GFSK, 920.9 MHz	150 kbps, ±37.5 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		41		dB
Selectivity, ±800 kHz, 150 kbps, ±37.5 kHz deviation, 2-GFSK, 920.9 MHz	150 kbps, ±37.5 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.9 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		47		dB
Sensitivity	200 kbps, ±50 kHz deviation, 2-GFSK, 918.4 MHz, 273 kHz RX BW, 10% PER, 250 byte payload		-99		dBm
Selectivity, ±400 kHz, 200 kbps, ±50 kHz deviation, 2-GFSK, 918.4 MHz	200 kbps, ±50 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 918.4 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		42		dB
Selectivity, ±800 kHz, 200 kbps, ±50 kHz deviation, 2-GFSK, 918.4 MHz	200 kbps, ±50 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 918.4 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		49		dB
Sensitivity	200 kbps, ±100 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.8 MHz, 10% PER, 250 byte payload		-99		dBm
Selectivity, ±600 kHz, 200 kbps, ±100 kHz deviation, 2-GFSK, 920.8 MHz	200 kbps, ±100 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.8 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		45		dB
Selectivity, ±1200 kHz, 200 kbps, ±100 kHz deviation, 2-GFSK, 920.8 MHz	200 kbps, ±100 kHz deviation, 2-GFSK, 273 kHz RX Bandwidth, 920.8 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		52		dB
Sensitivity	300 kbps, ±75 kHz deviation, 2-GFSK, 917.6 MHz, 498 kHz RX BW, 10% PER, 250 byte payload		-97		dBm
Selectivity, ±600 kHz, 300 kbps, ±75 kHz deviation, 2-GFSK, 917.6 MHz	300 kbps, ±75 kHz deviation, 2-GFSK, 498 kHz RX Bandwidth, 917.6 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		42		dB
Selectivity, ±1200 kHz, 300 kbps, ±75 kHz deviation, 2-GFSK, 917.6 MHz	300 kbps, ±75 kHz deviation, 2-GFSK, 498 kHz RX Bandwidth, 917.6 MHz, 10% PER, 250 byte payload. Wanted signal 3 dB above sensitivity level		47		dB

(1) Wanted signal 3 dB above the reference sensitivity limit according to ETSI EN 300 220 v. 3.1.1

8.11 861 MHz to 1054 MHz - Transmit (TX)

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled using 2-GFSK, 50 kbps, ±25 kHz deviation unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power, boost mode		VDDR = 1.95 V Minimum supply voltage (VDDS) for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Max output power		868 MHz and 915 MHz		13		dBm
Output power programmable range		868 MHz and 915 MHz		24		dB
Output power variation over temperature		+10 dBm setting Over recommended temperature operating range		±2		dB
Output power variation over temperature Boost mode		+14 dBm setting Over recommended temperature operating range		±1.5		dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) (2)	30 MHz to 1 GHz	+14 dBm setting ETSI restricted bands		< -54		dBm
		+14 dBm setting ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+14 dBm setting measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Spurious emissions out-of-band, 915 MHz (2)	30 MHz to 88 MHz (within FCC restricted bands)	+14 dBm setting		< -56		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	+14 dBm setting		< -52		dBm
	216 MHz to 960 MHz (within FCC restricted bands)	+14 dBm setting		< -50		dBm
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	+14 dBm setting		<-42		dBm
	1 GHz to 12.75 GHz (outside FCC restricted bands)	+14 dBm setting		< -40		dBm
Spurious emissions out-of-band, 920.6/928 MHz (2)	Below 710 MHz (ARIB T-108)	+14 dBm setting		< -36		dBm
	710 MHz to 900 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	900 MHz to 915 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	930 MHz to 1000 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	1000 MHz to 1215 MHz (ARIB T-108)	+14 dBm setting		< -45		dBm
	Above 1215 MHz (ARIB T-108)	+14 dBm setting		< -30		dBm
Harmonics	Second harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Third harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		
	Fourth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Fifth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		
Adjacent Channel Power						
Adjacent channel power, regular 14 dBm PA	Adjacent channel, 20 kHz offset. 9.6 kbps, h=0.5	12.5 dBm setting. 868.3 MHz. 14 kHz channel BW		-23		dBm

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled using 2-GFSK, 50 kbps, ±25 kHz deviation unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Alternate channel power, regular 14 dBm PA	Alternate channel, 40 kHz offset. 9.6 kbps, h=0.5	12.5 dBm setting. 868.3 MHz. 14 kHz channel BW		-30		dBm

(1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
(2) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

8.12 861 MHz to 1054 MHz - PLL Phase Noise Wideband Mode

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 20 kHz PLL loop bandwidth	±10 kHz offset		–76		dBc/Hz
	±100 kHz offset		–98		dBc/Hz
	±200 kHz offset		–106		dBc/Hz
	±400 kHz offset		–113		dBc/Hz
	±1000 kHz offset		–122		dBc/Hz
	±2000 kHz offset		–130		dBc/Hz
	±10000 kHz offset		–140		dBc/Hz

8.13 861 MHz to 1054 MHz - PLL Phase Noise Narrowband Mode

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 150 kHz PLL loop bandwith	±10 kHz offset		–95		dBc/Hz
	±100 kHz offset		–94		dBc/Hz
	±200 kHz offset		–94		dBc/Hz
	±400 kHz offset		–103		dBc/Hz
	±1000 kHz offset		–119		dBc/Hz
	±2000 kHz offset		–129		dBc/Hz
	±10000 kHz offset		–138		dBc/Hz

8.14 359 MHz to 527 MHz - Receive (RX)

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Spurious emissions 25 MHz to 1 GHz	433.92 MHz Conducted emissions measured according to ETSI EN 300 220		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		dBm
IEEE 802.15.4, 50 kbps, ±25 kHz Deviation, 2-GFSK, 78 kHz RX Bandwidth					
Sensitivity	BER = $10^{–2}$, 433.92 MHz		–110		dBm
Saturation limit	BER = $10^{–2}$, 433.92 MHz		10		dBm
Selectivity, +200 kHz	BER = $10^{–2}$, 433.92 MHz(1)		48		dB
Selectivity, -200 kHz	BER = $10^{–2}$, 433.92 MHz(1)		43		dB
Selectivity, +400 kHz	BER = $10^{–2}$, 433.92 MHz(1)		53		dB
Selectivity, -400 kHz	BER = $10^{–2}$, 433.92 MHz(1)		44		dB
Blocking, +1 MHz	BER = $10^{–2}$, 433.92 MHz(1)		60		dB
Blocking, -1 MHz	BER = $10^{–2}$, 433.92 MHz(1)		54		dB
Blocking, +2 MHz	BER = $10^{–2}$, 433.92 MHz(1)		62		dB
Blocking, -2 MHz	BER = $10^{–2}$, 433.92 MHz(1)		61		dB
Blocking, +10 MHz	BER = $10^{–2}$, 433.92 MHz(1)		75		dB
Blocking, -10 MHz	BER = $10^{–2}$, 433.92 MHz(1)		75		dB
Image rejection (image compensation enabled)	BER = $10^{–2}$, 433.92 MHz(1)		44		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
200 kbps, ±50 kHz Deviation, 2-GFSK, 273 kHz RX Bandwidth					
Sensitivity	BER = $10^{–2}$, 433.92 MHz		–104		dBm
Saturation limit	BER = $10^{–2}$, 433.92 MHz		10		dBm
Selectivity, ±400 kHz	BER = $10^{–2}$, 433.92 MHz(1)		48		dB
Blocking, ±1 MHz	BER = $10^{–2}$, 433.92 MHz(1)		52		dB
Blocking, ±2 MHz	BER = $10^{–2}$, 433.92 MHz(1)		55		dB
Blocking, ±10 MHz	BER = $10^{–2}$, 433.92 MHz(1)		68		dB
Image rejection (image compensation enabled)	BER = $10^{–2}$, 433.92 MHz(1)		45		dB
RSSI dynamic range	Starting from the sensitivity limit		89		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
SimpleLink™ Long Range, 2.5/5 kbps (20 ksps), ±5 kHz Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = $10^{–2}$, 433.92 MHz		-121		dBm
Sensitivity	5 kbps, BER = $10^{–2}$, 433.92 MHz		-119		dBm
Saturation limit	5 kbps, BER = $10^{–2}$, 433.92 MHz		10		dBm
Selectivity, +100 kHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		55		dB
Selectivity, -100 kHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		53		dB
Blocking, +1 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		69		dB
Blocking, -1 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		65		dB
Blocking, +2 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		71		dB
Blocking, -2 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		70		dB
Blocking, +10 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		84		dB
Blocking, -10 MHz	5 kbps, BER = $10^{–2}$, 433.92 MHz(1)		84		dB
Image rejection (image compensation enabled)	5 kbps, BER = $10^{–2}$, 433.92 MHz		49		dB
RSSI dynamic range	Starting from the sensitivity limit		101		dB

When measured on the CC1311-R3EM-5XD7793 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB

(1) Wanted signal 3 dB above sensitivity limit

8.15 359 MHz to 527 MHz - Transmit (TX)

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power		433.92 MHz, without BOOST (VDDR = 1.7 V)		13		dBm
Output power programmable range		433.92 MHz, without BOOST (VDDR = 1.7 V)		24		dB
Output power variation over temperature		+13 dBm setting. 433.92 MHz Over recommended temperature operating range		±1.5		dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) (2)	30 MHz to 1 GHz	+10 dBm setting ETSI restricted bands		< -54		dBm
		+10 dBm setting ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+10 dBm setting measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Spurious emissions out-of-band, 429 MHz (2)	Outside the necessary requency band (ARIB T-67)	+10 dBm setting		< -26		dBm
	710 MHz to 900 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	900 MHz to 915 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	930 MHz to 1000 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	1000 MHz to 1215 MHz (ARIB T-67)	+10 dBm setting		< -45		dBm
	Above 1215 MHz (ARIB T-67)	+10 dBm setting		< -30		dBm
Harmonics	Second harmonic	+13 dBm setting, 433 MHz		< -36		dBm
Harmonics	Third harmonic	+13 dBm setting, 433 MHz		< -30		dBm
Harmonics	Fourth harmonic	+13 dBm setting, 433 MHz		< -30		dBm
Harmonics	Fifth harmonic	+13 dBm setting, 433 MHz		< -30		dBm

(1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
(2) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

8.16 359 MHz to 527 MHz - PLL Phase Noise

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 433 MHz band 20 kHz PLL loop bandwidth	±10 kHz offset		-82		dBc/Hz
	±100 kHz offset		-105		dBc/Hz
	±200 kHz offset		-112		dBc/Hz
	±400 kHz offset		-119		dBc/Hz
	±1000 kHz offset		-127		dBc/Hz
	±2000 kHz offset		-133		dBc/Hz
	±10000 kHz offset		-141		dBc/Hz

8.17 Timing and Switching Characteristics

8.17.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.17.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active(1)			850 - 4000		µs
MCU, Shutdown to Active(1)			850 - 4000		µs
MCU, Standby to Active			160		µs
MCU, Active to Standby			36		µs
MCU, Idle to Active			14		µs

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

8.17.3 Clock Specifications

8.17.3.1 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ≤ 9 pF		20	60	Ω
ESR	Equivalent series resistance 5 pF < C_L ≤ 6 pF			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)(5)		$< 3 \times 10^{-25} / C_L{}^2$		H
C_L	Crystal load capacitance(4)	5	7(3)	9	pF
	Start-up time(2)		200		µs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
(5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.17.3.2 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

8.17.3.3 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	kΩ
C_L	Crystal load capacitance	6	7(1)	12	pF

(1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.17.3.4 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Calibrated frequency			32.8		kHz
Calibrated RTC variation(1)	Calibrated periodically against XOSC_HF(2)		±600(3)		ppm
Temperature coefficient.			50		ppm/°C

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
(2) TI driver software calibrates the RTC every time XOSC_HF is enabled.
(3) Some device's variation can exceed 1000 ppm. Further calibration will not improve variation.

8.17.4 Synchronous Serial Interface (SSI) Characteristics

8.17.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	System Clocks (2)
S2(1)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3(1)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams Figure 8-1, Figure 8-2, and Figure 8-3.
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

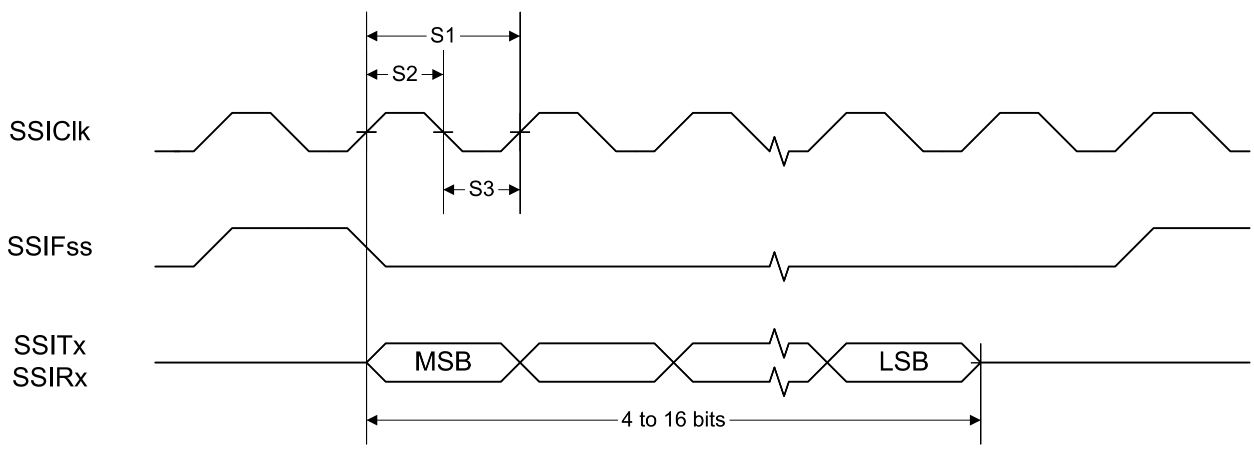

Figure 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

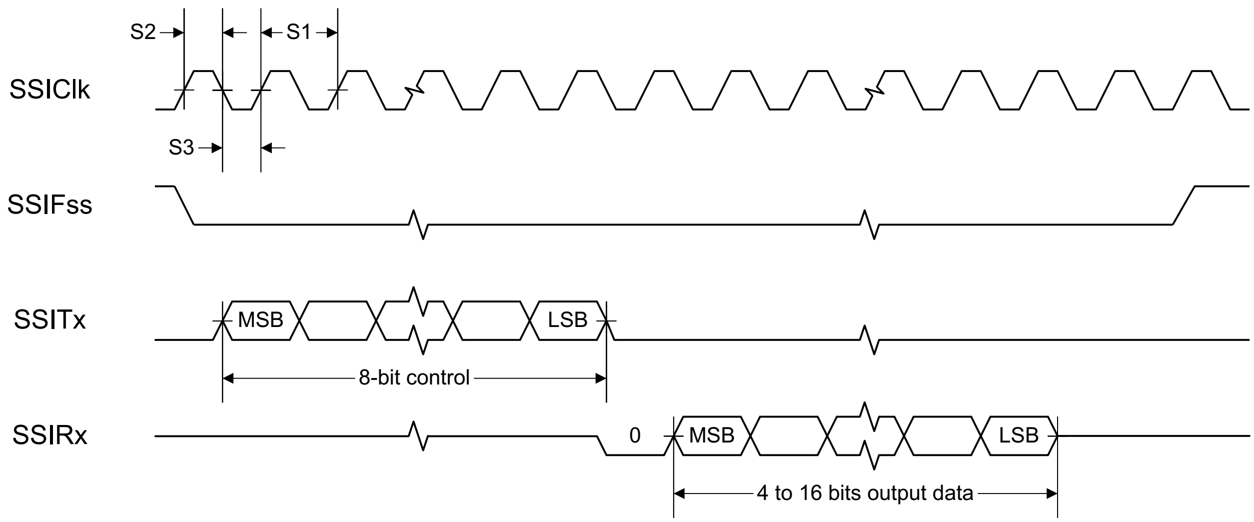

Figure 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

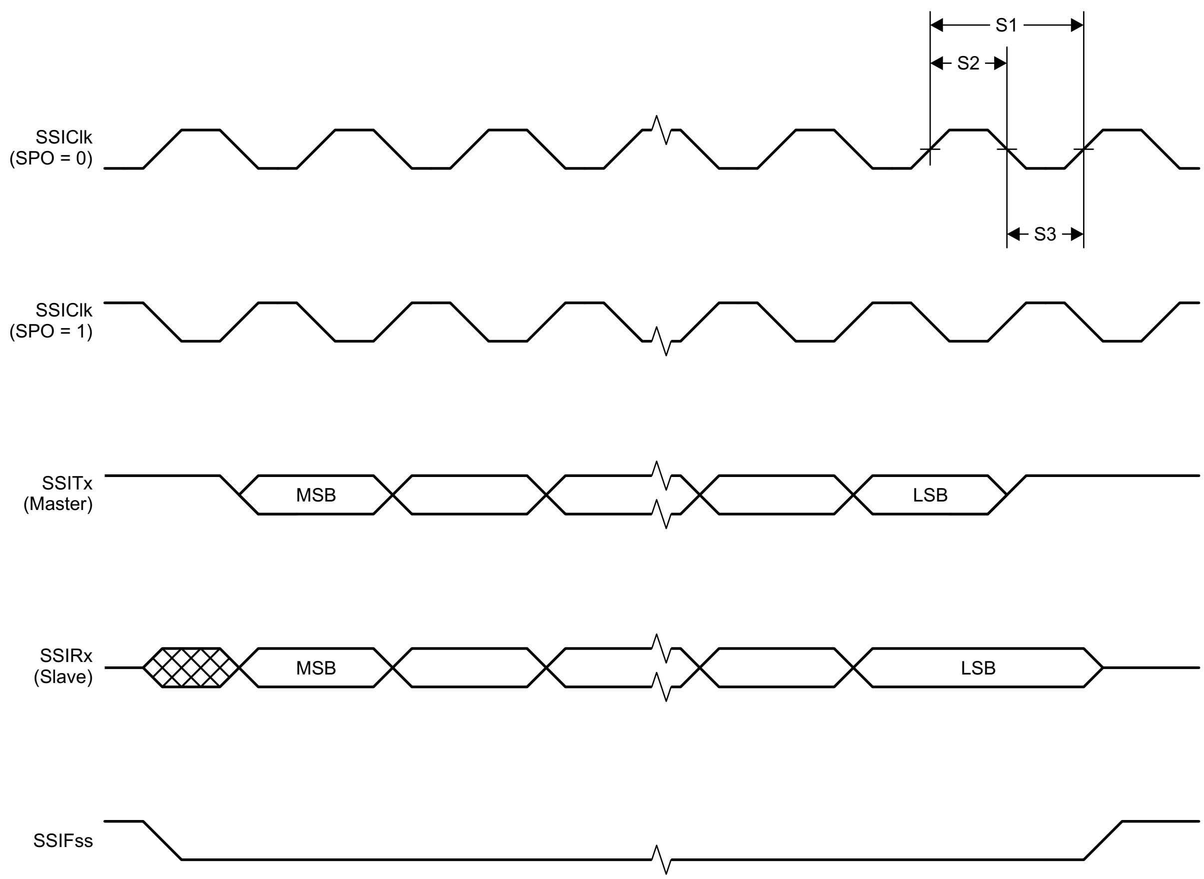

Figure 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.17.5 UART

8.17.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

8.18 Peripheral Characteristics

8.18.1 ADC

8.18.1.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.[(1)]
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample Rate				200	ksps
	Offset	Internal 4.3 V equivalent reference[(2)]		–0.24		LSB
	Gain error	Internal 4.3 V equivalent reference[(2)]		7.14		LSB
DNL[(4)]	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference[(2)], 200 kSamples/s, 9.6 kHz input tone		9.8		Bits
		Internal 4.3 V equivalent reference[(2)], 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled		9.8		
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		10.1		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		11.1		
		Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone [(5)]		11.3		
		Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone [(5)]		11.6		
THD	Total harmonic distortion	Internal 4.3 V equivalent reference[(2)], 200 kSamples/s, 9.6 kHz input tone		–65		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		–70		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference[(2)], 200 kSamples/s, 9.6 kHz input tone		60		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		63		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference[(2)], 200 kSamples/s, 9.6 kHz input tone		70		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		73		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24 MHz clock		50		Clock Cycles
	Current consumption	Internal 4.3 V equivalent reference[(2)]		0.39		mA
	Current consumption	VDDS as reference		0.56		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/ offset compensation factors stored in FCFG1		4.3[(2)] [(3)]		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference, input voltage scaling enabled		VDDS		V
	Reference voltage	VDDS as reference, input voltage scaling disabled		VDDS / 2.82[(3)]		V

8.18.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.[1]
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings at all times
(4) No missing codes
(5) ADC_output = $\Sigma(4^n$ samples) >> n, n = desired extra bits

8.18.2 DAC

8.18.2.1 Digital-to-Analog Converter (DAC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution			8		Bits
V_{DDS}	Supply voltage	Any load, any V_{REF}, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load[4], any V_{REF}, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	
		Any load, V_{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F_{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V_{REF} = VDDS, buffer OFF, internal load		13		1 / F_{DAC}
		V_{REF} = VDDS, buffer ON, external capacitive load = 20 pF[3]		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			MΩ
	Short circuit current				400	µA
Z_{MAX}	Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz	VDDS = 3.8 V, DAC charge-pump OFF		50.8		kΩ
		VDDS = 3.0 V, DAC charge-pump ON		51.7		
		VDDS = 3.0 V, DAC charge-pump OFF		53.2		
		VDDS = 2.0 V, DAC charge-pump ON		48.7		
		VDDS = 2.0 V, DAC charge-pump OFF		70.2		
		VDDS = 1.8 V, DAC charge-pump ON		46.3		
		VDDS = 1.8 V, DAC charge-pump OFF		88.9		
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator						
DNL	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 250 kHz		±1		LSB[1]
	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 16 kHz		±1.2		
	Offset error[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±0.64		LSB[1]
		V_{REF} = VDDS= 3.0 V		±0.81		
		V_{REF} = VDDS = 1.8 V		±1.27		
		V_{REF} = DCOUPL, pre-charge ON		±3.43		
		V_{REF} = DCOUPL, pre-charge OFF		±2.88		
		V_{REF} = ADCREF		±2.37		

8.18.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error(2) Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±0.78		LSB(1)
		V_{REF} = VDDS = 3.0 V		±0.77		
		V_{REF} = VDDS= 1.8 V		±3.46		
		V_{REF} = DCOUPL, pre-charge ON		±3.44		
		V_{REF} = DCOUPL, pre-charge OFF		±4.70		
		V_{REF} = ADCREF		±4.11		
	Max code output voltage variation(2) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±1.53		LSB(1)
		V_{REF} = VDDS = 3.0 V		±1.71		
		V_{REF} = VDDS= 1.8 V		±2.10		
		V_{REF} = DCOUPL, pre-charge ON		±6.00		
		V_{REF} = DCOUPL, pre-charge OFF		±3.85		
		V_{REF} = ADCREF		±5.84		
	Max code output voltage variation(2) Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±2.92		LSB(1)
		V_{REF} =VDDS= 3.0 V		±3.06		
		V_{REF} = VDDS= 1.8 V		±3.91		
		V_{REF} = DCOUPL, pre-charge ON		±7.84		
		V_{REF} = DCOUPL, pre-charge OFF		±4.06		
		V_{REF} = ADCREF		±6.94		
	Output voltage range(2) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.62		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.86		
		V_{REF} = VDDS= 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
	Output voltage range(2) Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS= 3.8 V, code 255		3.61		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS = 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
External Load (Keysight 34401A Multimeter)						
INL	Integral nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB(1)
		V_{REF} = DCOUPL, F_{DAC} = 250 kHz		±1		
		V_{REF} = ADCREF, F_{DAC} = 250 kHz		±1		
DNL	Differential nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB(1)

8.18.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error	V_{REF} = VDDS= 3.8 V		±0.20		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.25		
		V_{REF} = VDDS = 1.8 V		±0.45		
		V_{REF} = DCOUPL, pre-charge ON		±1.55		
		V_{REF} = DCOUPL, pre-charge OFF		±1.30		
		V_{REF} = ADCREF		±1.10		
	Max code output voltage variation	V_{REF} = VDDS= 3.8 V		±0.60		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.55		
		V_{REF} = VDDS= 1.8 V		±0.60		
		V_{REF} = DCOUPL, pre-charge ON		±3.45		
		V_{REF} = DCOUPL, pre-charge OFF		±2.10		
		V_{REF} = ADCREF		±1.90		
	Output voltage range Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.61		
		V_{REF} = VDDS = 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS= 1.8 V, code 1		0.02		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.02		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.20		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.02		
		V_{REF} = ADCREF, code 255		1.42		

(1) 1 LSB (V_{REF} 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter

8.18.3 Temperature and Battery Monitor

8.18.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		°C
Accuracy	-40 °C to 0 °C		±4.0		°C
Accuracy	0 °C to 105 °C		±2.5		°C
Supply voltage coefficient(1)			3.9		°C/V

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

8.18.3.2 Battery Monitor

Measured on a Texas Instruments reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
Integral nonlinearity (max)			23		mV
Accuracy	VDDS = 3.0 V		22.5		mV
Offset error			-32		mV
Gain error			-1		%

8.18.4 Comparator

8.18.4.1 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range(1)		0		V_{DDS}	V
Offset	Measured at V_{DDS} / 2		±5		mV
Decision time	Step from –10 mV to 10 mV		0.78		µs
Current consumption	Internal reference		9.2		µA

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.18.5 GPIO

8.18.5.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V

8.18.5.1 GPIO DC Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

8.19 Typical Characteristics

All measurements in this section are done with T_c = 25 °C and V_{DDS} = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions*, Section 8.3, for device limits. Values exceeding these limits are for reference only.

8.19.1 MCU Current

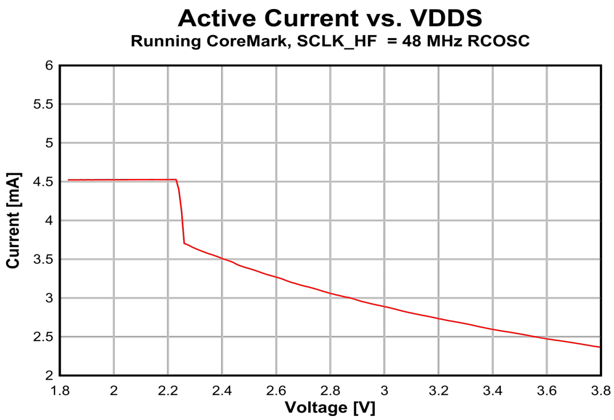

Figure 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)

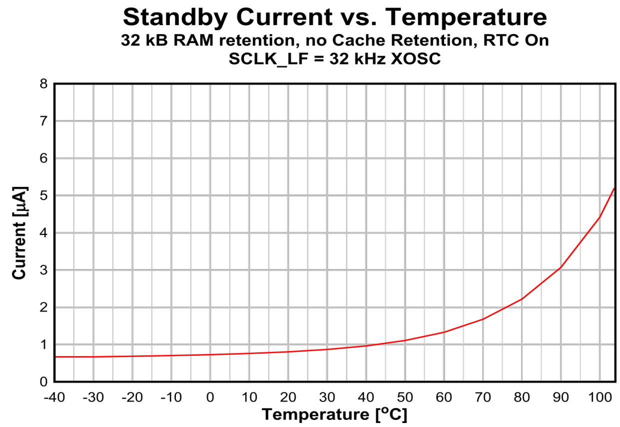

Figure 8-5. Standby Mode (MCU) Current vs. Temperature

8.19.2 RX Current

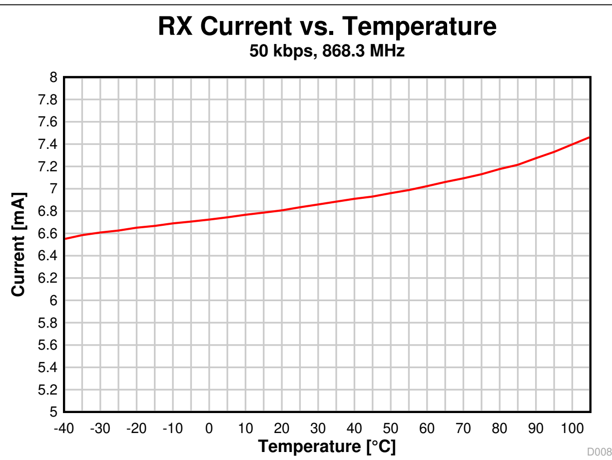

Figure 8-6. RX Current vs. Temperature (50 kbps, 868.3 MHz)

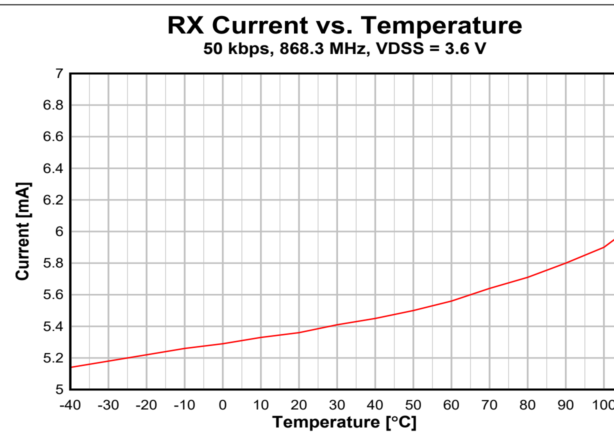

Figure 8-7. RX Current vs. Temperature (50 kbps, 868.3 MHz, VDDS = 3.6 V)

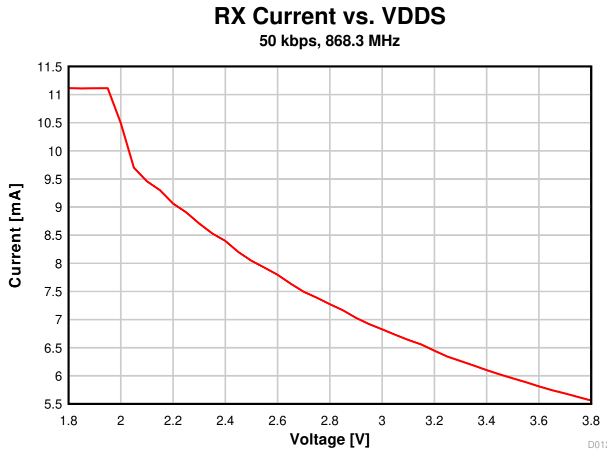

Figure 8-8. RX Current vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

8.19.3 TX Current

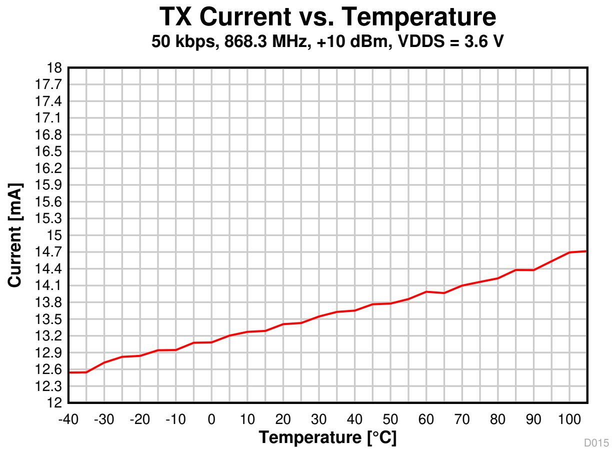

Figure 8-9. TX Current vs. Temperature (50 kbps, 868.3 MHz, VDDS = 3.6 V)

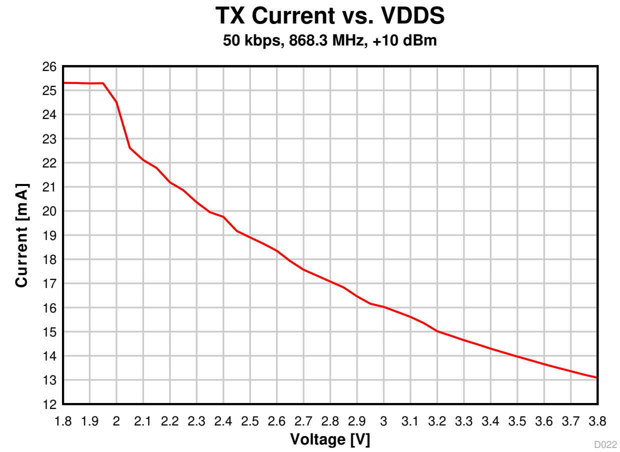

Figure 8-10. TX Current vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

Table 8-1 shows typical TX current and output power for different output power settings.

Table 8-1. Typical TX Current and Output Power, regular PA (915 MHz, VDDS = 3.0 V)

CC1311R3 at 915 MHz, VDDS = 3.0 V (Measured on CC1311-R3EM-5XD7793)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x013F[1]	14	14.3	30.5
0xB224	12.5	12.6	22.3
0x895E	12	12.1	20.8
0x669A	11	11.0	18.7
0x3E92	10	10.0	16.9
0x3EDC	9	9.0	15.9
0x2CD8	8	8.4	15.1
0x26D4	7	7.5	14.0
0x20D1	6	6.5	13.0
0x1CCE	5	5.2	11.9
0x16CD	4	4.6	11.5
0x14CB	3	3.4	10.6
0x12CA	2	2.6	10.2
0x12C9	1	1.8	9.7
0x10C8	0	0.8	9.3
0xAC4	-5	-5.1	7.2
0xAC2	-10	-10.6	6.2
0x6C1	-15	-14.9	5.7
0x4C0	-20	-21.0	5.2

[1] Boost mode enabled. VDDR regulated to 1.95 V.

8.19.4 RX Performance

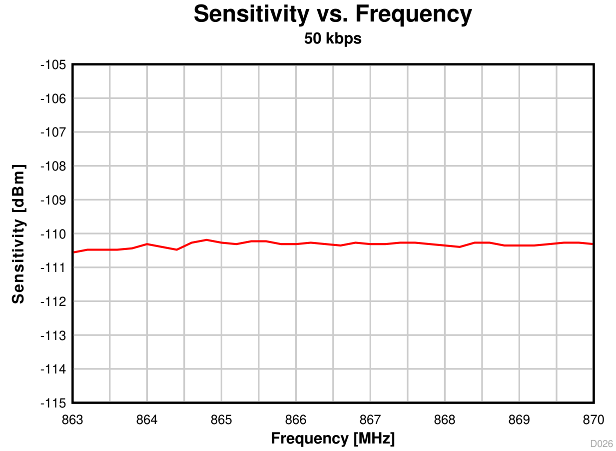

Figure 8-11. Sensitivity vs. Frequency (50 kbps, 868 MHz)

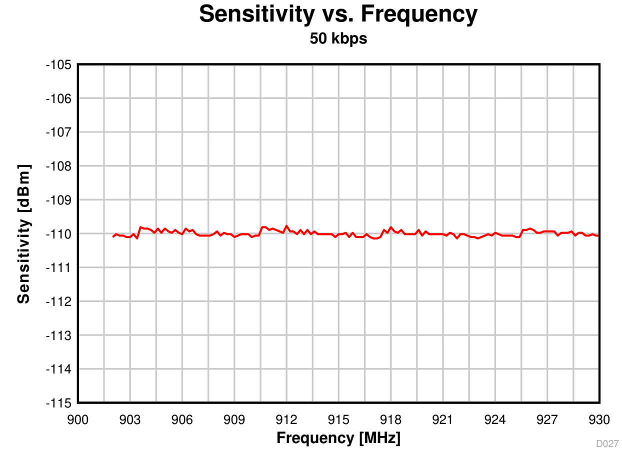

Figure 8-12. Sensitivity vs. Frequency (50 kbps, 915 MHz)

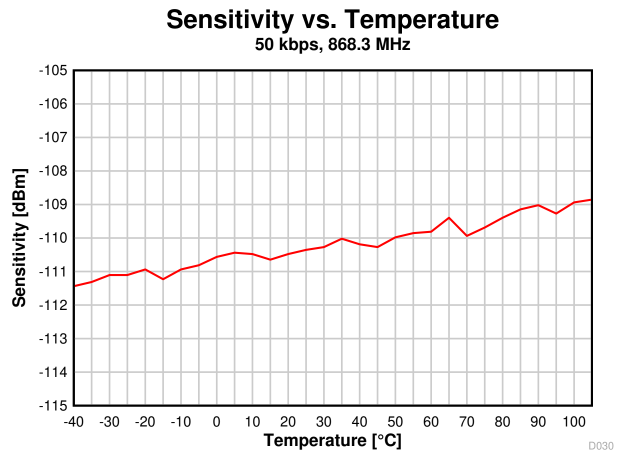

Figure 8-13. Sensitivity vs. Temperature (50 kbps, 868.3 MHz)

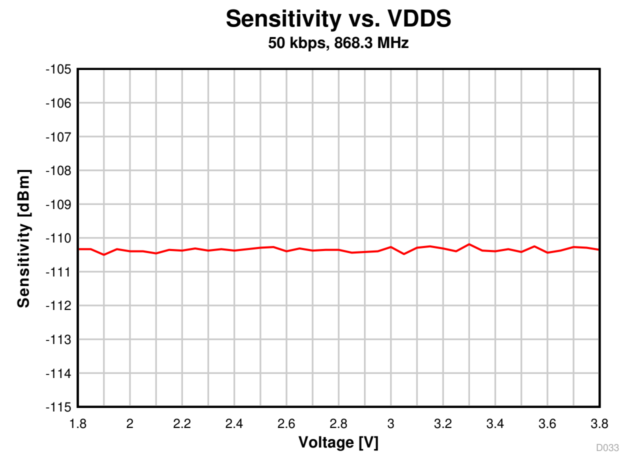

Figure 8-14. Sensitivity vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

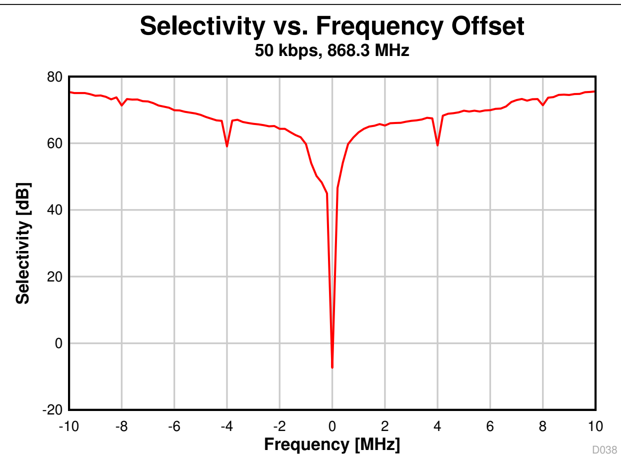

Figure 8-15. Selectivity vs. Frequency Offset (50 kbps, 868.3 MHz)

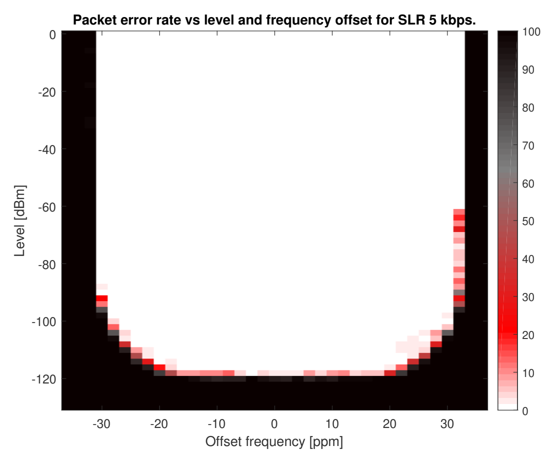

Figure 8-16. PER vs. Level vs. Frequency (SimpleLink™ Long Range 5 kbps, 868 MHz)

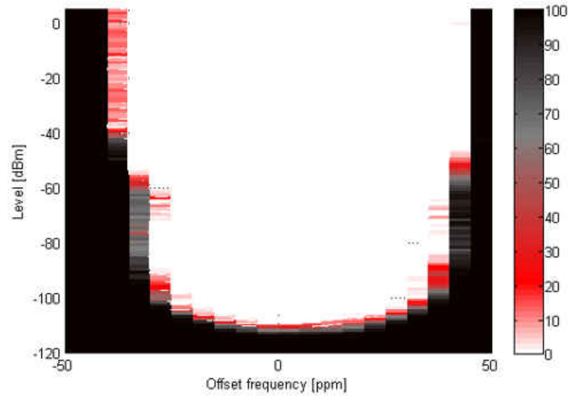

Figure 8-17. 802.15.4, 50 kbps, ±25 kHz deviation, 2-GFSK, 100 kHz RX Bandwidth

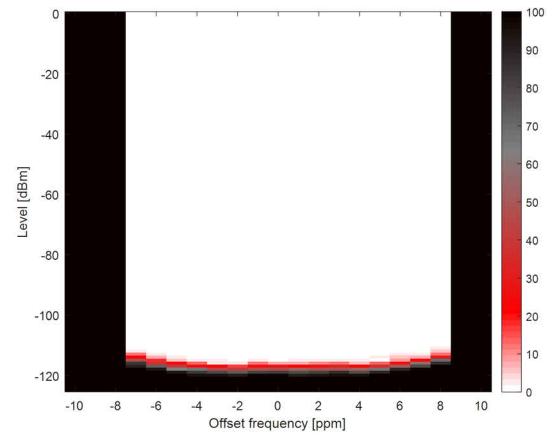

Figure 8-18. Narrowband, 9.6 kbps ±2.4 kHz deviation, 2-GFSK, 868 MHz, 17.1 kHz RX Bandwidth

8.19.5 TX Performance

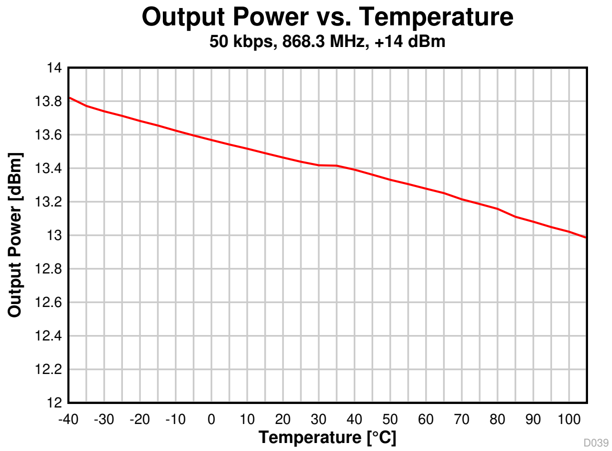

Figure 8-19. Output Power vs. Temperature (50 kbps, 868.3 MHz)

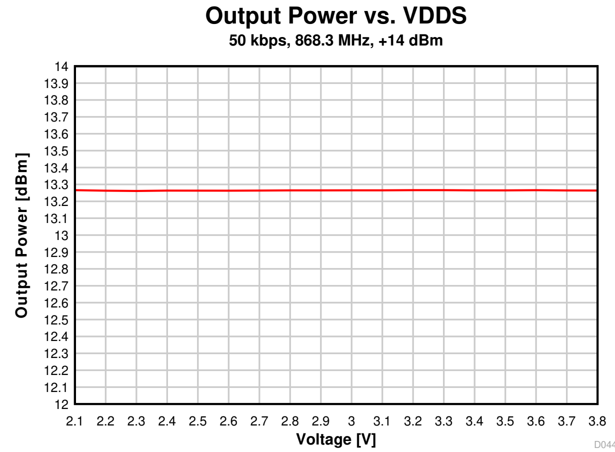

Figure 8-20. Output Power vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

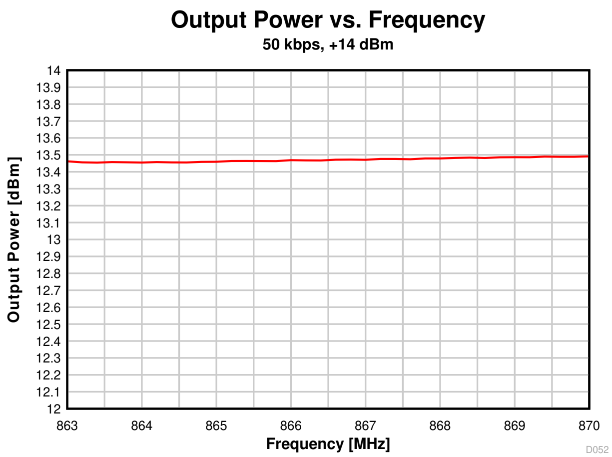

Figure 8-21. Output Power vs. Frequency (50 kbps, 868 MHz)

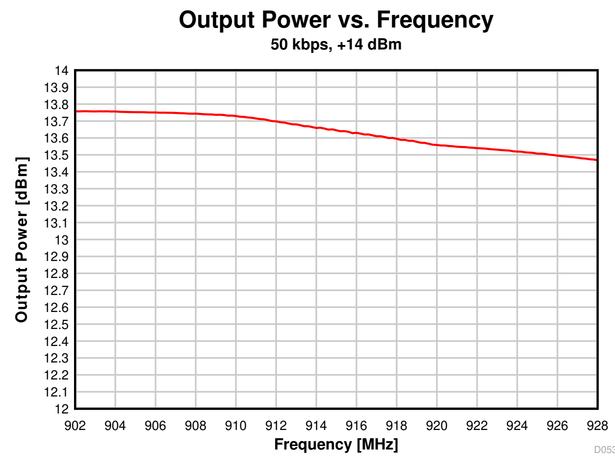

Figure 8-22. Output Power vs. Frequency (50 kbps, 915 MHz)

8.19.6 ADC Performance

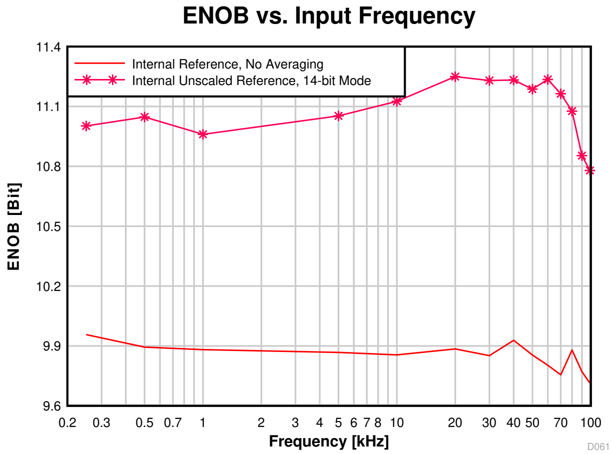

Figure 8-23. ENOB vs. Input Frequency

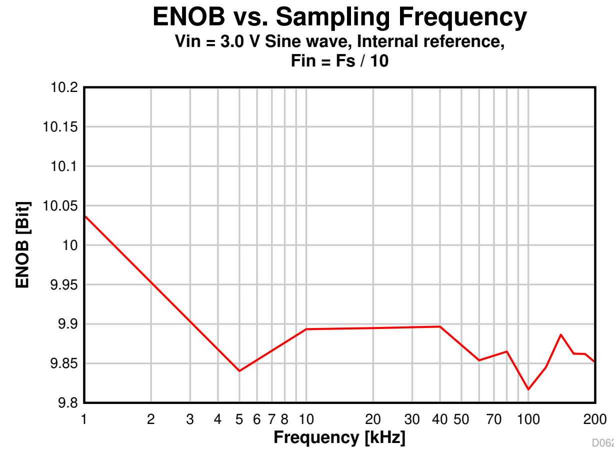

Figure 8-24. ENOB vs. Sampling Frequency

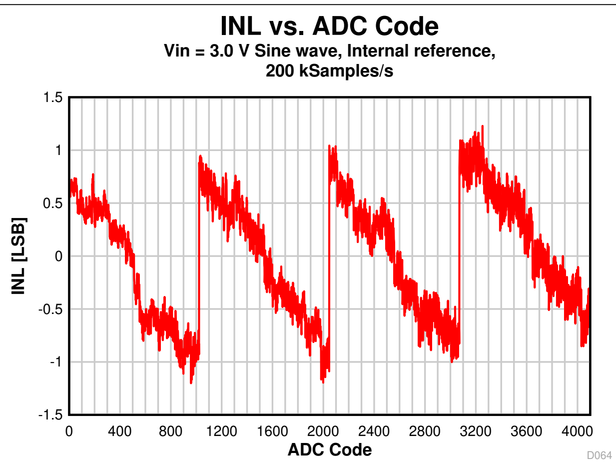

Figure 8-25. INL vs. ADC Code

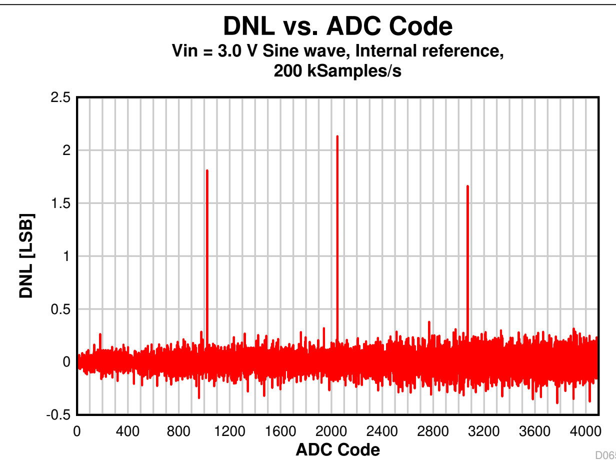

Figure 8-26. DNL vs. ADC Code

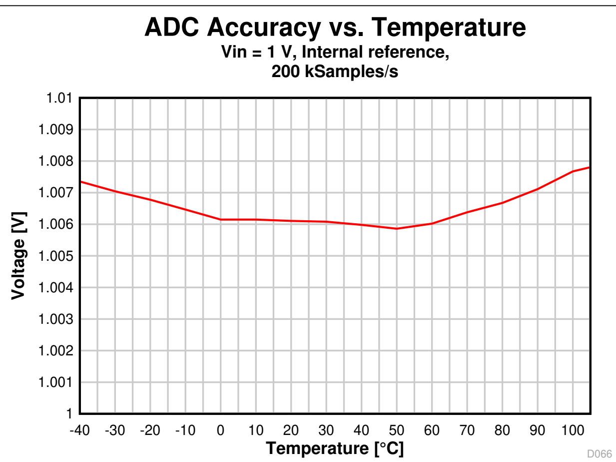

Figure 8-27. ADC Accuracy vs. Temperature

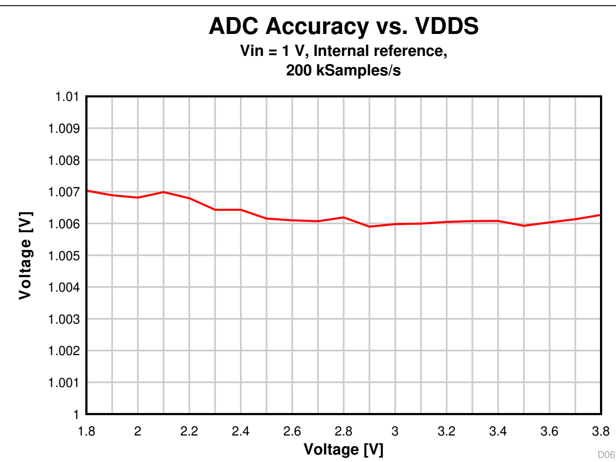

Figure 8-28. ADC Accuracy vs. Supply Voltage (VDDS)

9 Detailed Description

9.1 Overview

Section 4 shows the core modules of the CC1311R3 device.

9.2 System CPU

The CC1311R3 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4 system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

Note

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the SmartRF Studio tool with performance numbers of selected formats found in Section 8.

9.3.1 Proprietary Radio Formats

The CC1311R3 radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

Table 9-1 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

Table 9-1. Feature Support

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Programmable preamble, sync word and CRC	Yes	Yes	Yes	No
Programmable receive bandwidth	Yes	Yes	Yes (down to 4 kHz)	Yes
Data / Symbol rate(3)	20 to 1000 kbps	≤ 2 Msps	≤ 100 ksps	≤ 20 ksps
Modulation format	2-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK
Dual Sync Word	Yes	Yes	No	No
Carrier Sense (1) (2)	Yes	No	No	No
Preamble Detection(2)	Yes	Yes	Yes	No
Data Whitening	Yes	Yes	Yes	Yes
Digital RSSI	Yes	Yes	Yes	Yes
CRC filtering	Yes	Yes	Yes	Yes
Direct-sequence spread spectrum (DSSS)	No	No	No	1:2 1:4 1:8
Forward error correction (FEC)	No	No	No	Yes
Link Quality Indicator (LQI)	Yes	Yes	Yes	Yes

(1) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD_PROP_CS radio API.
(2) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.
(3) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.

9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is a single 32-KB block and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

The ROM contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Cryptography

The CC1311R3 device comes with a wide set of cryptography-related hardware accelerators, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.

The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Advanced Encryption Standard (AES)** with 128 bit key lengths

Together with the hardware accelerator module, a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The TI provided cryptography drivers are:

- **Key Agreement Schemes**
  – Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
- **Signature Generation**
  – Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  – Short Weierstrass form (full hardware support), such as:
    - NIST-P256
  – Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **Hash**
  – SHA256
- **MACs**
  – HMAC with SHA256
  – AES CBC-MAC
- **Block ciphers**
  – AESECB
  – AESCBC
  – AESCTR
- **Authenticated Encryption**
  – AESCCM
- **Random number generation**
  – True Random Number Generator
  – AES CTR DRBG

9.6 Timers

A large selection of timers are available as part of the CC1311R3 device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)
  This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

9.7 Serial Peripherals and I/O

The SSI is a synchronous serial interface that is compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSI support both SPI master and slave up to 4 MHz. The SSI module support configurable phase and polarity.

The UART implement universal asynchronous receiver and transmitter functions. It support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x1x3, CC26x1x3 SimpleLink™ Wireless MCU Technical Reference Manual.

9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1311R3 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

9.11 Power Management

To minimize power consumption, the CC1311R3 supports a number of power modes and power management features (see Table 9-2).

Table 9-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 9-2).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

Note

The power, RF and clock management for the CC1311R3 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1311R3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.12 Clock Systems

The CC1311R3 device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC1311R3 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

For general design guidelines and hardware configuration guidelines, refer to CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report.

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC1311R3 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

CC1311-R3EM-5XD7793 Design Files The CC1311-R3EM-5XD7793 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This reference design is intended for operation in the 868 MHz and 915 MHz bands.

LP-CC1311P3 Design Files The CC1311P3 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC1311P3 device. This LaunchPad is intended for operation in the 868 MHz and 915 MHz bands.

Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

10.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are three recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\text{JT}} \times P + T_{\text{case}} \tag{1}$$

2. From board temperature:

$$T_J = \psi_{\text{JB}} \times P + T_{\text{board}} \tag{2}$$

3. From ambient temperature:

$$T_J = R_{\theta\text{JA}} \times P + T_A \tag{3}$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

Example:

Using Equation 3, the temperature difference between ambient temperature and junction temperature is calculated. In this example, we assume a simple use case where the radio is transmitting continuously at 10 dBm output power. Let us assume the ambient temperature is 85°C and the supply voltage is 3.6 V. To calculate P, we need to look up the current consumption for Tx at 85°C in Figure 8-9. From the plot, we see that the current consumption is 14.4 mA. This means that P is 14.4 mA × 3.6 V = 51.8 mW.

The junction temperature is then calculated as:

$$T_J = 23.4^{\circ C}/_{W} \times 51.8mW + T_A = 1.2°C + T_A \tag{4}$$

As can be seen from the example, the junction temperature is 1.2 °C higher than the ambient temperature when running continuous Tx at 85°C and, thus, well within the recommended operating conditions.

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, etc. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in Measuring CC13xx and CC26xx current consumption.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC1311R3 is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC1311R3* devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

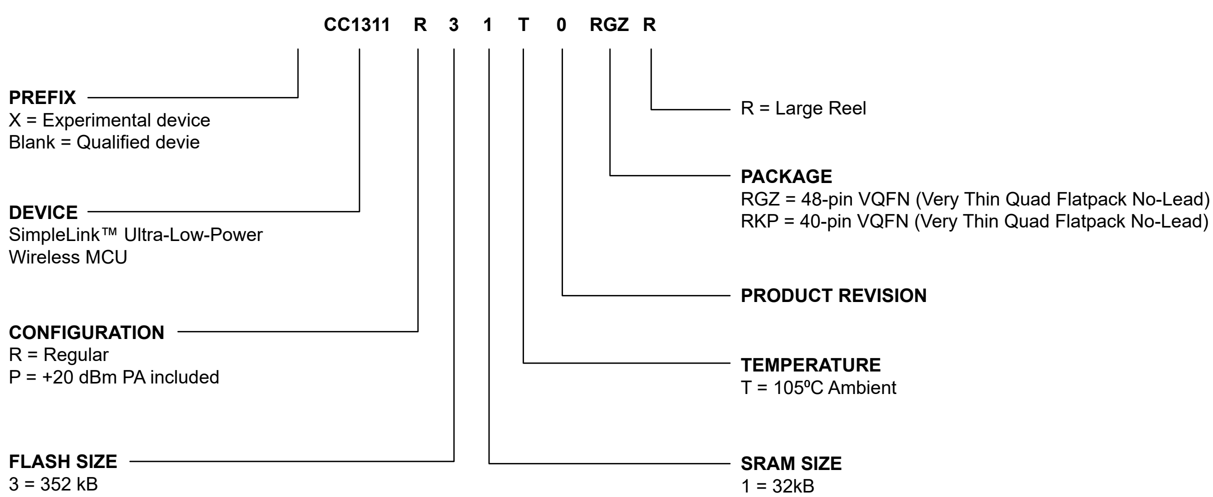

Figure 11-1. Device Nomenclature

11.2 Tools and Software

The CC1311R3 device is supported by a variety of software and hardware development tools.

Development Kit

CC1311P3 LaunchPad™ Development Kit

The CC1311P3 LaunchPad™ Development Kit enables development of high-performance Sub-1 GHz wireless applications that benefit from low-power operation. The kit features the CC1311P3 Sub-1 GHz SimpleLink Wireless MCU. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more.

Software

SimpleLink™ CC13XX-CC26XX SDK

The SimpleLink CC13xx and CC26xx Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC1311R3 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- Wi-SUN®
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- Proprietary RF - a large set of building blocks for building proprietary RF software
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13XX-CC26XX SDK is part of TI’s SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit http://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

11.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC1311R3. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer — Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC1311R3 Silicon Errata — The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC1311R3 device are found on the device product folder at: ti.com/product/CC1311R3/#tech-docs.

Technical Reference Manual (TRM)

CC13x1x, CC26x1x SimpleLink™ Wireless MCU TRM — The TRM provides a detailed description of all modules and peripherals available in the device family.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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Eclipse® is a registered trademark of Eclipse Foundation.
IAR Embedded Workbench® is a registered trademark of IAR Systems AB.
Windows® is a registered trademark of Microsoft Corporation.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1311R31T0RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC1311 R31	Samples
CC1311R31T0RKPR	ACTIVE	VQFN	RKP	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC1311 R31	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

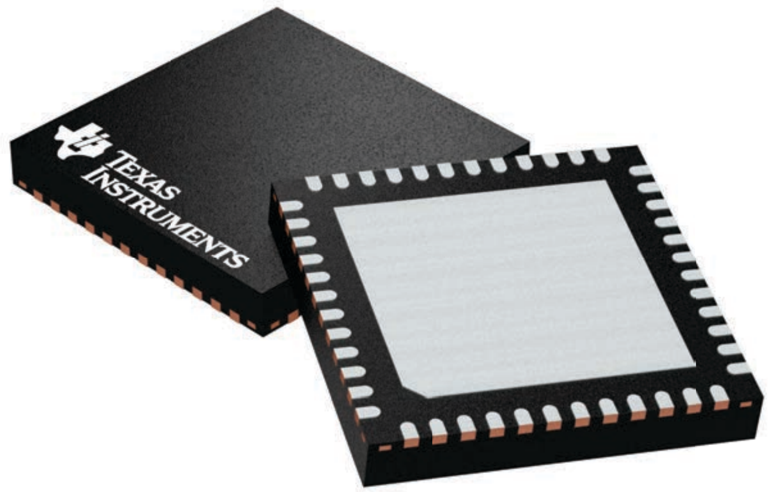
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGZ 48

VQFN - 1 mm max height

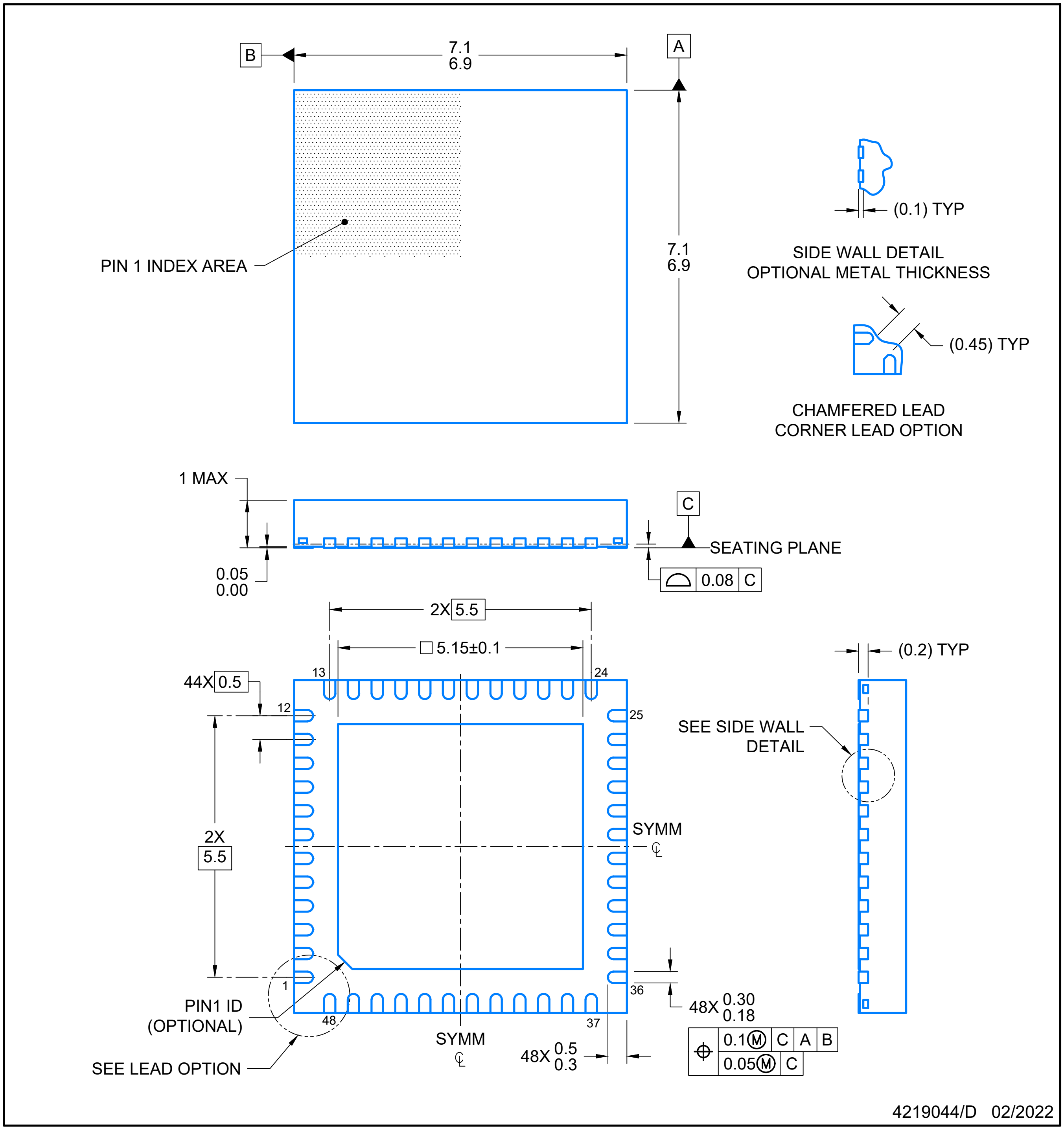
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



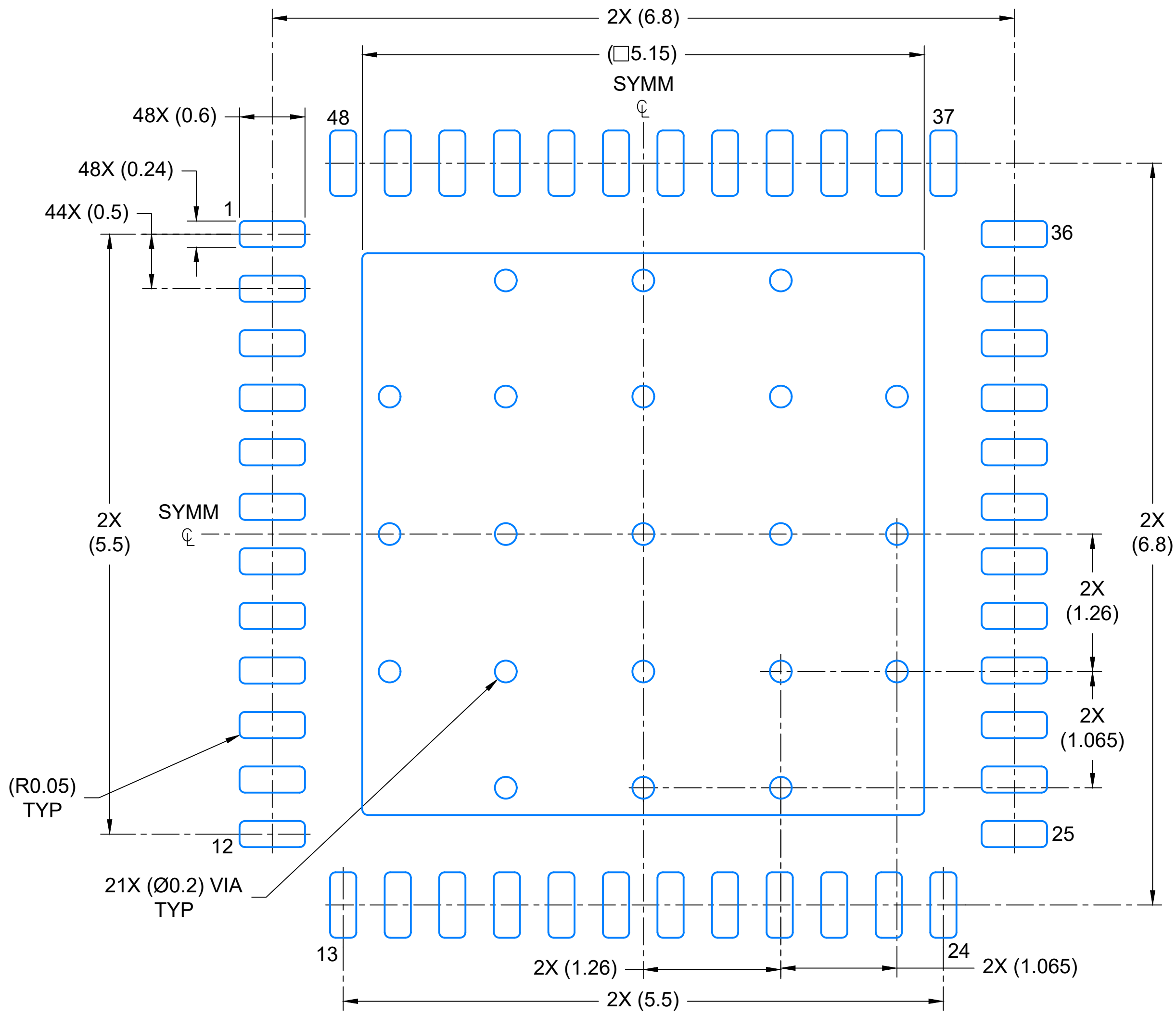
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



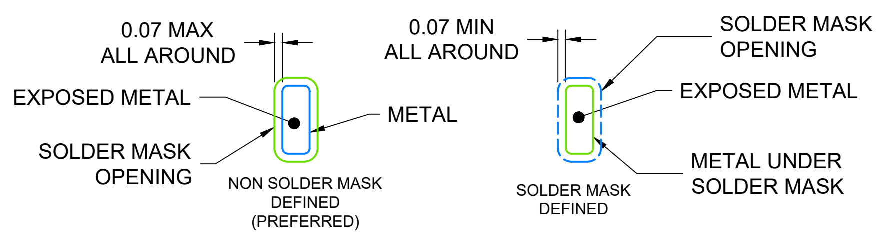
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

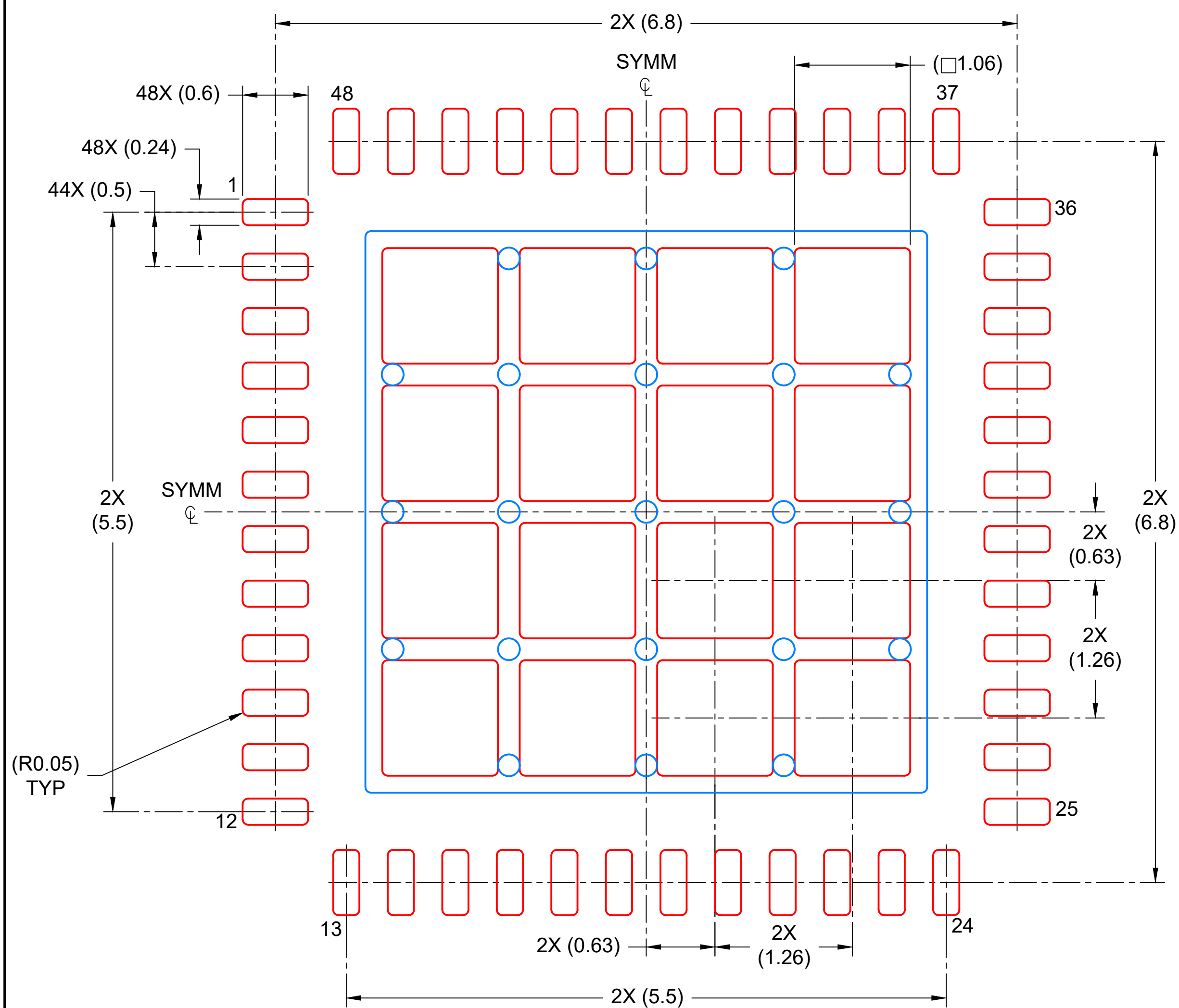


SOLDER MASK DETAILS

4219044/D 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

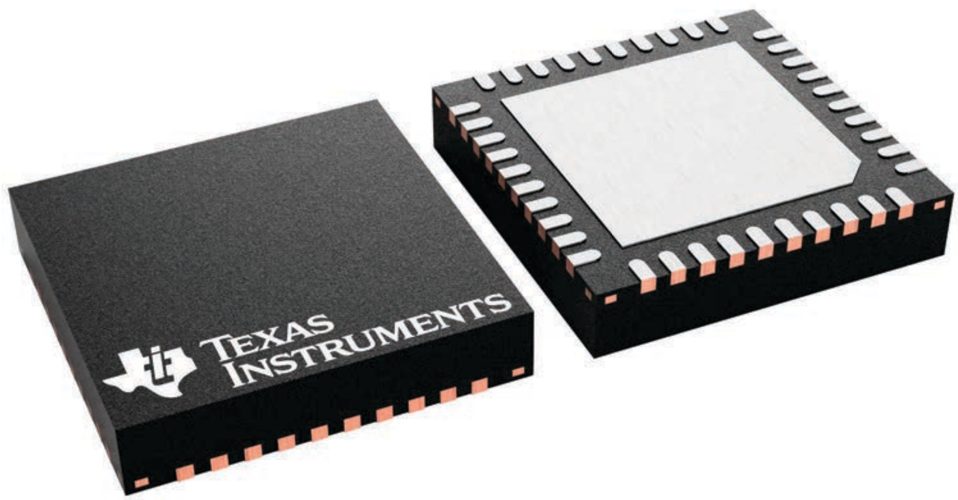
EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

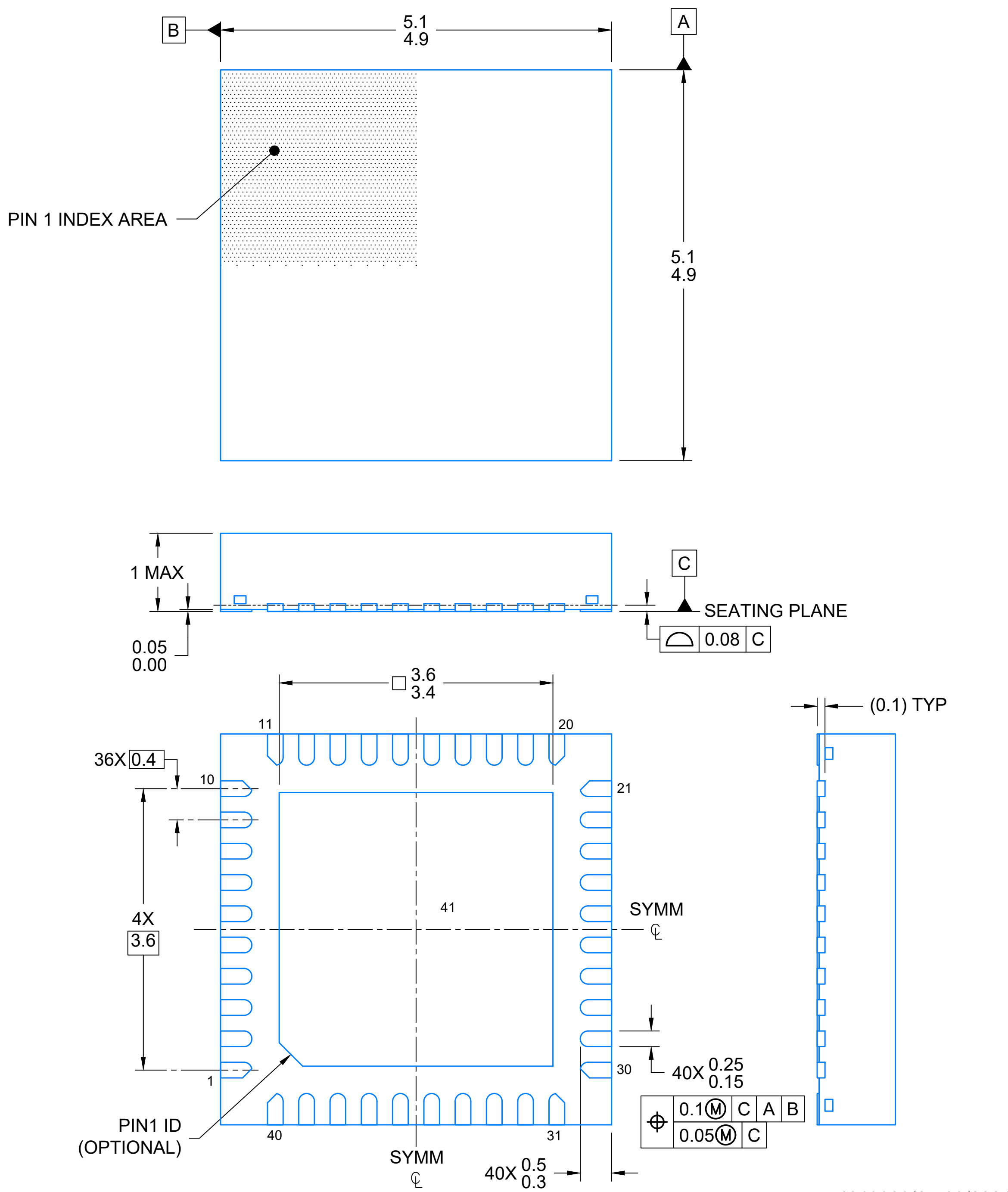
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



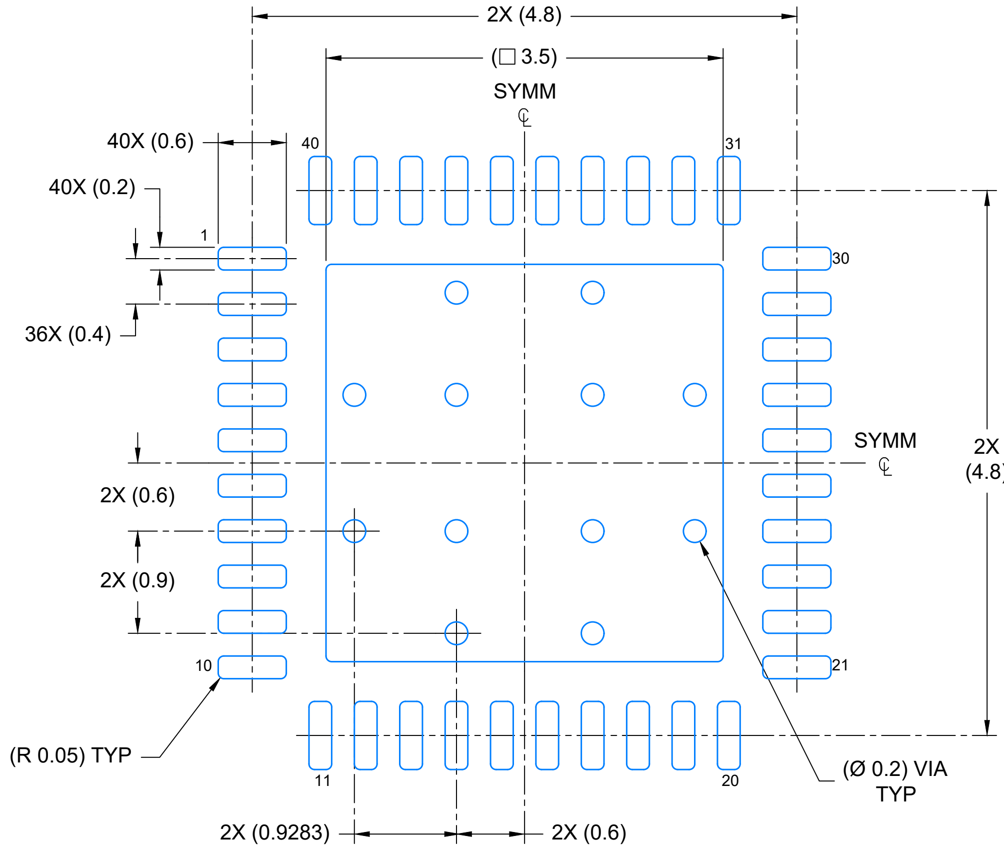
4229305/A



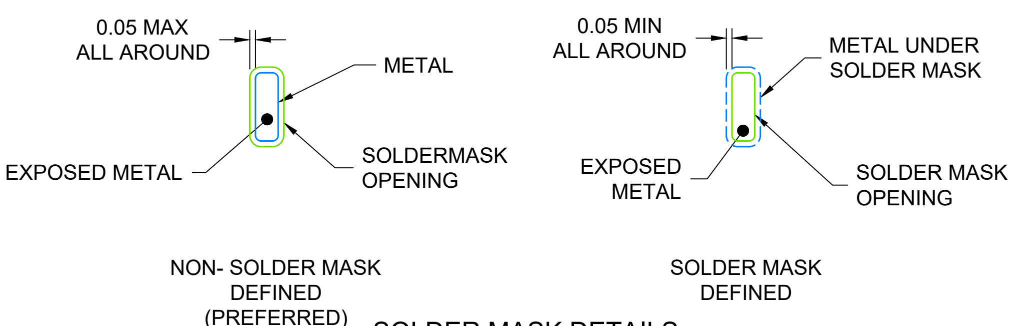
4219083/A 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

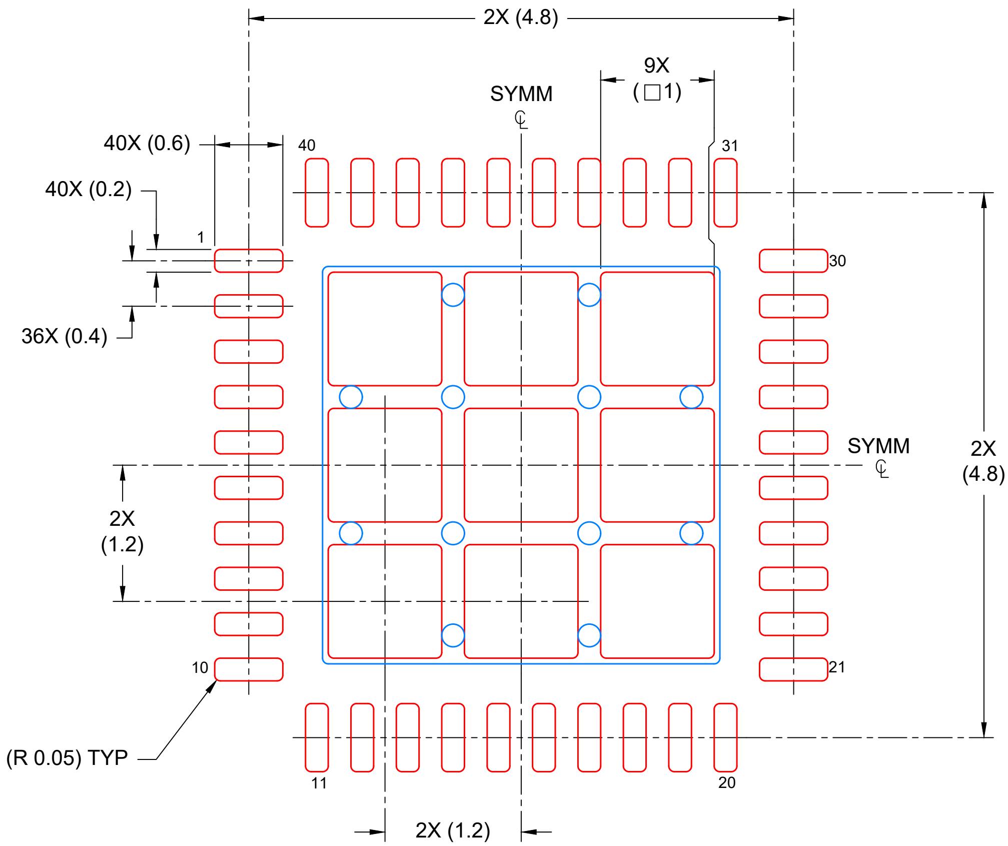


SOLDER MASK DETAILS

4219083/A 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 15X

4219083/A 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.